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TECHNICAL/APPLICATIONS SECTION

DEPARTMENTS

ON THE COVER: The variety of applications for a new generation of hyperabrupt GaAs tuning varactors is shown in the illustration by Bob Shoof. Artwork courtesy of M/A-COM Gallium Arsenide Products, Inc. See the Technical Feature beginning on page 99.

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A New Approach to FET Power Amplifiers

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Introduction

Current and projected military and commercial systems require FET power amplifiers with ever increasing output power and efficiency at higher operating frequencies. In an effort to meet these demands, device designers have pushed the performance of the GaAs FET nearly to its limit. Further significant device improvements must be accompanied by improved circuit techniques. Conventional circuit techniques are simply inadequate when applied to the problem of high efficiency FET cell combining at Ku-band and higher frequencies. This paper will describe a unique chip-level cell combining technique that has demonstrated, as a 6-cell combiner, a combining efficiency of greater than 90% at 15 GHz.

In order to realize significantly higher power levels with FET devices, some method of power combining is required. Since the breakdown voltage is limited by material constants, increased power levels are usually achieved by increasing the FET device size. However, the FET cell size is limited by several fundamental factors, including internal phasing and yield considerations. For example, at X-band frequencies, we have found that the individual cell size is limited to a total gate periphery of approximately 1200 μm. In general, larger cells result in low device gain, lower efficiency and lower output power density (W/mm of gate periphery). These problems increase with increasing frequency, further limiting the maximum FET cell size and power capability. Therefore, efficient cell combining techniques are required in order to realize larger higher power devices.

This work was supported in part by the U.S. Army Electronics Research and Development Command, Fort Monmouth, New Jersey, under contract DAAK20-80-C-0286.

Conventional Cell Combining Techniques

The cell combining problem is illustrated schematically in Figure 1 where an array of 6 cells are interfaced in some, as of yet undefined, manner to an external circuit. Typically, this problem has been addressed by simply paralleling the cells with bond wires,[1] thereby creating a larger device which is capable of higher power. While this technique is simple and works reasonably well at low frequencies, cell paralleling has the following fundamental problems:

- Unequal power levels at the cell sites which results from the lack of any systematic means of controlling the incident power density at the individual cell sites. A lower impedance cell will, consequently, receive more than its share of the input drive.
- Interaction between cells due to cell-to-cell parameter variation. The cell-to-cell imbalances result in high circulating currents which leads to high losses.
- Phasing and connection problems due to the cell array width approaching a significant fraction of a wavelength.
- Transverse propagating modes which can result when the cells are paralleled with non-zero length lines. This can, in turn, result in push-pull type oscillations between cells and often catastrophic failure.
- Low input-output impedance levels. The low impedance level results from the shunting effect of the paralleled cells. This, in turn, causes high matching circuit losses and potentially narrow bandwidth.

The net result of these problems is that cell paralleling is not a very attractive technique for combining a large number of cells at high frequencies.

Recently, lumped element cell combining techniques, adapted from bipolar power transistors at L- and S-band frequencies, have been applied to the problem of power FET cell combining at X-band frequencies[2,3]. While reasonably successful at 10 GHz and below, this method treats only the problem of low device impedance

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level by employing individual low-pass LC matching networks. The combiner circuit is purely reactive; no consideration is given to the problems of power sharing, phasing problems or transverse propagating modes. While an improvement over direct cell paralleling, it does not address the fundamental problems of cell combining.

The above combining techniques become inadequate when the combination of frequency and number of cells exceeds some limit. In general, the number of cells that can be combined successfully using conventional techniques decreases with increasing frequency. For cell combining at high frequencies, an approach is required which treats the cell combining problem as a circuit level power combining problem with integral cell isolation characteristics.

Chip-Level Cell Combiner

A new chip-level power combiner[4] has been developed to efficiently combine the device cell array. The approach is a planar version of the circuit-level radial line combiner.[5] A sketch of the approach as a 6-cell combiner is shown in Figure 2. As shown in the figure, the cell combiner is implemented directly on the chip carrier, resulting in a compact power FET structure with an active area of approximately 100 x 160 mils. The chip carrier consists of the FET cell array sandwiched between an input power divider

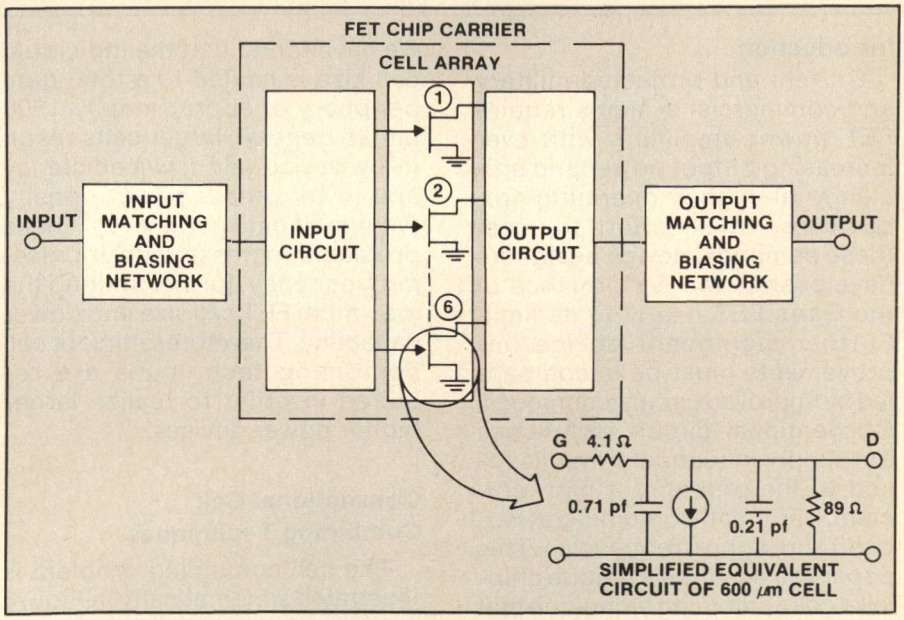

Fig. 1 FET cell combining problem.

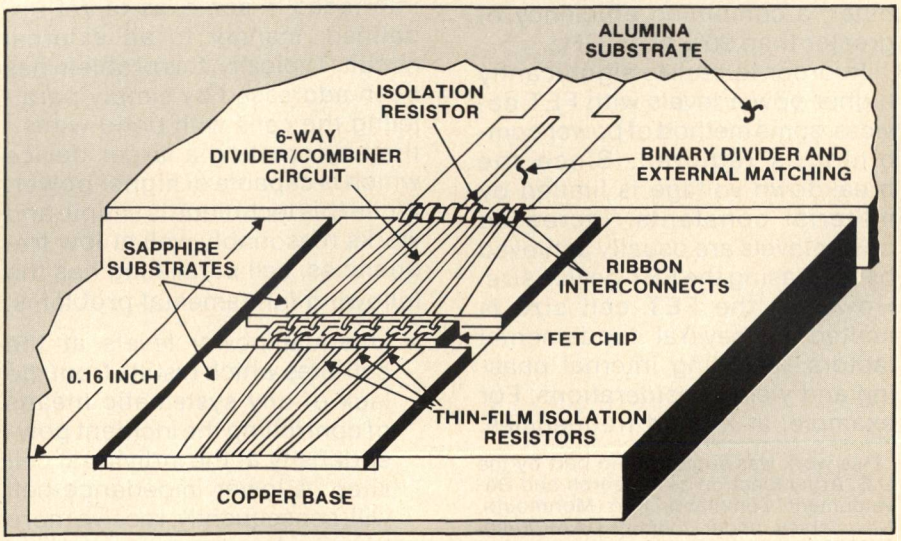

Fig. 2 Chip-level cell combining approach.

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and an output power combiner. The divider/combiner circuit consists of a 2-section cascade of a 2-segment and a 6-segment planar transmission line array. Each section is nominally 90° in electrical length at the design center frequency. The first 2-segment section, which is fabricated on a 25 mil thick alumina substrate, is also part of the external matching network. The second section, which consists of an array of six low impedance transmission lines and the five isolation resistors connecting between them, is fabricated on a thin sapphire substrate. The thin sapphire substrates are required in order to realize the low impedance transmission lines in a transverse dimension equal to the physical cell array width. This approach results in a uniform phase front with minimum phase error across the array due to width discontinuity.

The bond wires to the gate/drain pad are employed to effectively series resonate the cell input/output impedance at band center frequency. Additional matching and biasing networks, required to realize a complete amplifier, are external to the chip carrier. The divider/combiner circuits not only provide isolation between the combined cells, but also form impedance inverters transforming the low device impedance to a higher intermediate level. This power combining approach to cell combining has the following benefits:

- Facilitates combining an electrically large ($>\lambda/4$) arrays
- Results in isolation between cells and thereby tolerates significant cell to cell variation without interaction
- Due to the resistive isolation between cells, the transverse propagating modes are terminated; hence push-pull oscillations are suppressed.
- Exhibits graceful degradation characteristics
- The power combiner also serves as an impedance inverter transforming the low device impedance to a higher level.

The equivalent circuit of the chip-level power combiner is shown in Figure 3. The key element in this approach is the planar divider/combiner circuit. It consists of a 2-section cascade of transmission line segments with interconnecting isolation resistors. The distinguishing feature of this approach is that the isolation resistors connect between adjacent transmission line segments, as opposed to a common floating node as in the case of the N-way Wilkinson.[6] This isolation resistor configuration solves the topological problem created by the requirement for a common node in the Wilkinson approach and thereby permits a planar configuration. The transmission line sections (each 90° in length at midband) are specified to form a 2-section impedance transformer for the even mode, and the isolation resistors are specified to terminate the odd modes. The isolation resistors, while indicated with the same symbol in the figure, are not necessarily equal in value.

This chip-level approach is similar in concept to the circuit-level combiner proposed by Nagai, et. al.[7] The Nagai combiner scheme is shown schematically in Figure 4. This class of in-phase power combining circuits is characterized by an M-section cascade of N transmission line segments and M sets of interconnecting isolation resistors. In general, the Nagai approach requires N-1 sections (M=N-1) in order to insure that all possible modes, except for the desired even mode, are completely terminated. While theoretically correct, it may be impractical or even unnecessary to utilize the complete array of N-1 sections in order to fully terminate the N-1 independent odd modes. For example, if N=6, the Nagai combiner requires five $\lambda/4$ sections which is usually impractical. The resultant combiner structure would be excessively large and lossy. Clearly, from an efficiency and size point-of-view, only one or perhaps two $\lambda/4$ sections can be tolerated. While the 2-section combiner presented in this paper cannot fully terminate the five independent odd modes that a 6-way combiner can support, it can be shown theoretically that by proper choice of the isolation resistor values, the odd modes can be sufficiently termi-

[*Continued on page 56*]

nated. What this means is that the odd modes experience sufficient loss such that there is a minimum interaction between the six isolated ports. Only the desired even mode experiences no loss.

As opposed to the Nagai scheme, our approach does not require the parallel transmission line segments to be isolated. The proximity coupling effects between the parallel lines are included in the design. During the even mode excitation, the presence of adjacent lines increases the even mode impedance. Due to the absence of an adjacent line on the end segments, the end transmission lines exhibit a lower Z_o than the internal elements. This "end effect" is compensated by narrowing the end segments thereby raising their Z_o. During odd mode excitation, the presence of adjacent transmission lines lowers the effective Z_o of the lines. This, in turn, results in a somewhat reduced odd mode bandwidth. This is not a limitation for modest bandwidth (30-40%) applications.

Another novel aspect of this approach is the tapered transmission line segments. This accomplishes two major objectives:

- Permits the fanning out of the input line to the cell array width
- Provides first order phase compensation for the end transmission line segments.

A physically wide cell array is geometrically difficult to feed equally due to the relatively narrow input transmission lines (typically 0.025 inch wide for 50 ohm microstrip). This problem is solved by fanning out in 2 steps: first, in the 2-segment section, and then in the 6-segment section using the tapered transmission lines. This simultaneously produces a first order phase compensation for the end transmission line segments. Due to the absence of an adjacent line on the end segment, the waves on the end segments experience less dielectric slowing and propagate faster. The tapered transmission lines produce a longer path length for the outer segments, and therefore, the waves propagating on the parallel transmission line segments arrive in phase at the chip.

While the even mode properties

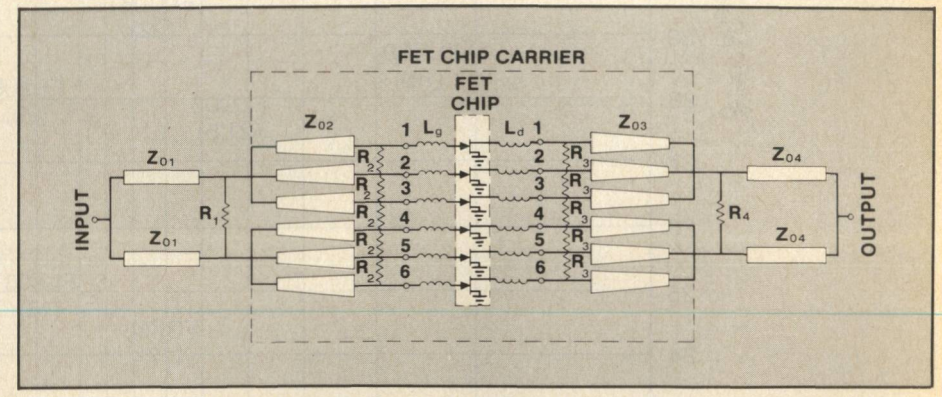

Fig. 3 Equivalent circuit of FET cell combiner.

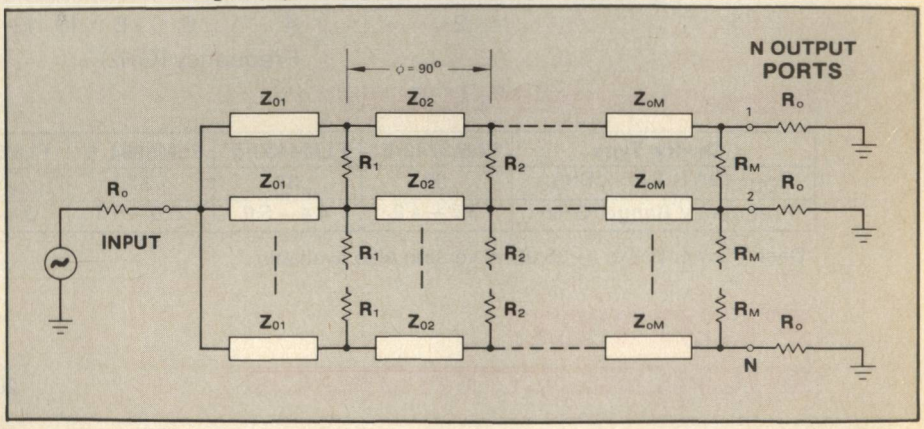

Fig. 4 Nagai N-way planar combining network.

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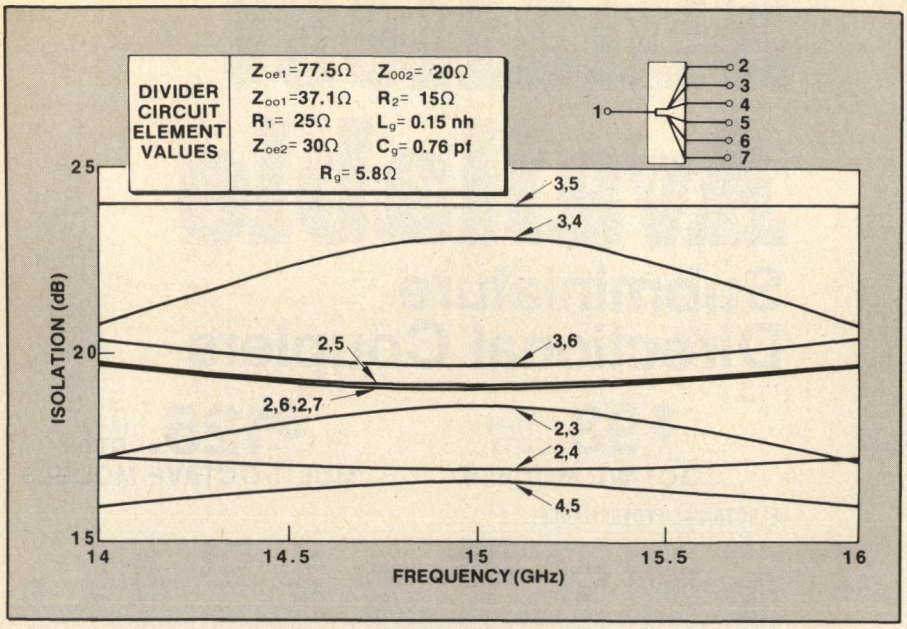

Fig. 5 Port-to-port isolation properties.

of this chip-level combiner are relatively easy to demonstrate experimentally, due to fixturing problems, the odd mode properties must be inferred from indirect measurements or from computer simulations. Therefore, in order to demonstrate the isolation properties of the combiner, we have simulated the 2-section input divider circuit, shown in Figure 3, on the computer. The input divider circuit together with the gate equivalent circuits of the six 600 μm cells are included. The results of the computer simulations over the 14 to 16 GHz frequency range are shown in Figure 5. This does not represent an optimized solution. We are still refining our combiner analysis and synthesis capabilities. All possible combinations are shown, and the minimum isolation between any two ports is 16 dB. In general, the isolation is poorest between adjacent ports and improves with port separation. With the exception of the port combinations 4-5, 2-4 and 2-3, the isolation is greater than 19 dB over the entire 14 to 16 GHz band.

FET Power Amplifier

Several single stage FET amplifier circuits have been fabricated and tested using this chip-level cell combining technique. Employing a 6-cell 3600 μm gate width device, we have achieved power levels as high as 2.3 watts at 15 GHz with 4.2 dB associated gain and efficiencies as high as 27.9%. This represents new state of the art performance levels for power FETs at this frequency. Due to the demonstrated high efficiency nature of this technique, it is particularly well suited for FET cell combining at Ku-band and higher frequencies where the combining losses of conventional techniques become unacceptable.

One of the key factors leading to the success of this effort was the treatment of the device-circuit problem as a single problem with the device specifically tailored to the chip-level combiner. As the frequency increases, it becomes more difficult to separate the device from the circuit. The FET

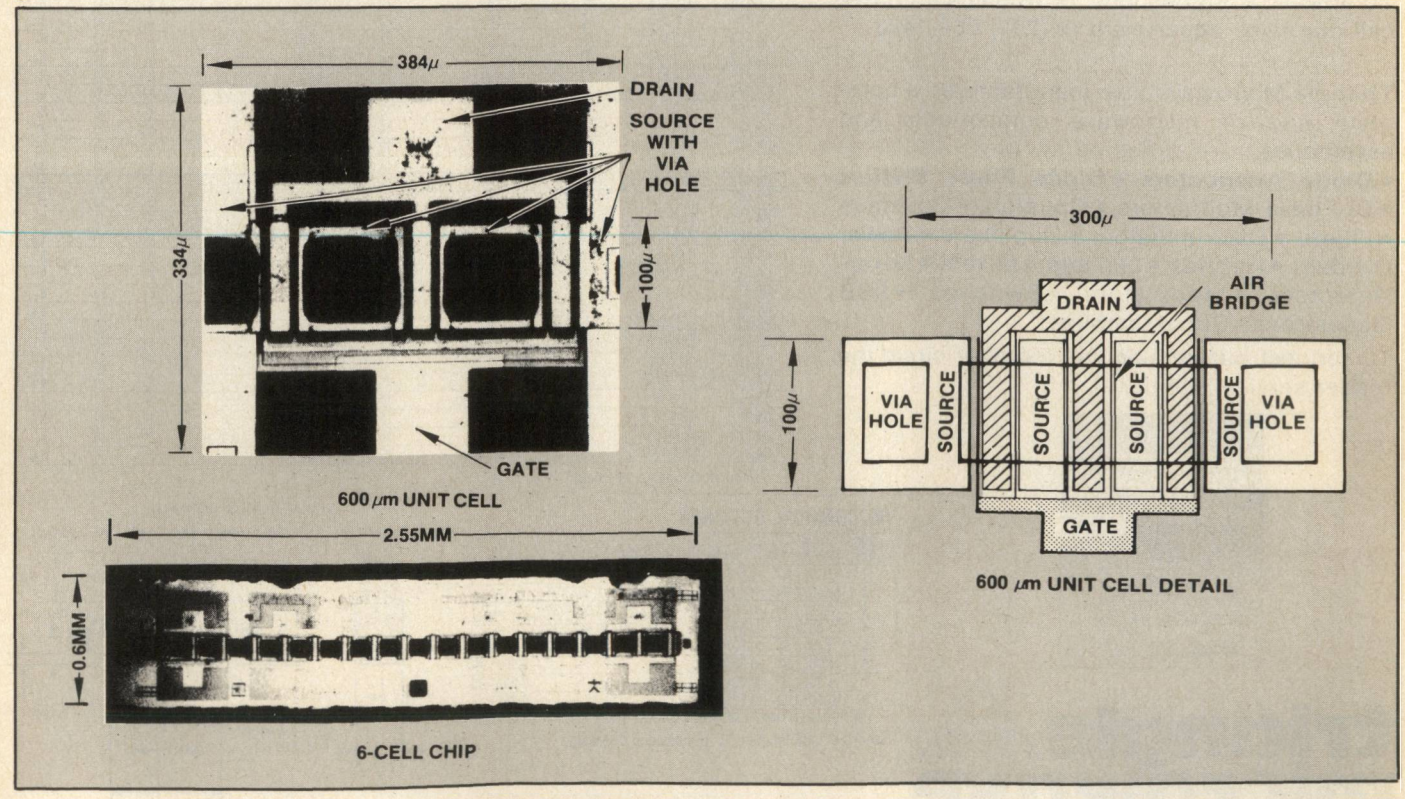

Fig. 6 6-Cell 3600 μm FET device geometry.

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device employed in the combiner consists of a 6-cell array of 600 μm unit cells with a low density of gate periphery per unit length in the transverse direction. A photograph of the device is shown in Figure 6, and the device design is described in detail in reference 8. The low gate density results in improved device thermal impedance (and hence improved reliability) and lower effective source inductance. In addition, from a matching network point-of-view, the wide array configuration is advantageous since it allows the array to be fed by a lower impedance transmission line. This, in turn, results in greater bandwidth capability.

A photograph of the hybrid chip-level power combiner is shown in Figure 7. It consists of the 6-cell FET chip mounted between two sapphire substrates on a copper base. The substrates are soldered to the base using an Au-Ge eutectic solder, while the FET chip is soldered to the base with an Au-Sn eutectic solder. The overall dimensions of the carrier are 0.16 x 0.3 x 0.025 inch. The 0.025 inch dimension is required to make the carrier compatible with conventional 0.025 inch microstrip circuits without further discontinuities in the ground plane.

Sapphire was selected as the substrate material due to its low loss properties, high dielectric constant, excellent surface finish and rugged mechanical properties. Also it is available in thicknesses as small as 0.001 inch. Thin-film isolation resistors were fabricated on the sapphire substrates by sputtering tantalum nitride.

The low impedance section adjacent to the FET is required to match the low input/output impedance of the FET. For a 6-cell array of 600 μm cells, the total input impedance is approximately 0.7Ω. In order to match this low impedance level with minimum bandwidth/loss degradation, a transmission line inverter with a Z_o of less than 4Ω is required. This extraordinarily low impedance level can only be achieved by employing very high w/h ratios (30 to 40) which in turn requires

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very thin substrates. Figure 8 illustrates the characteristic impedance and corresponding element Q of a microstrip transmission line for large w/h ratios with the line wide "w" fixed at 68 mils (the average width of the low impedance section). The dielectric constant of 9.4 assumes a sapphire substrate with the c-axis in the plane of the substrate. The plot indicates that low Z_o levels can be achieved with reasonable Q values. For example, with a substrate thickness of 2 mils (w/h=34) a Z_o of 3.4Ω can be achieved with a corresponding Q of 92. For comparison, typical

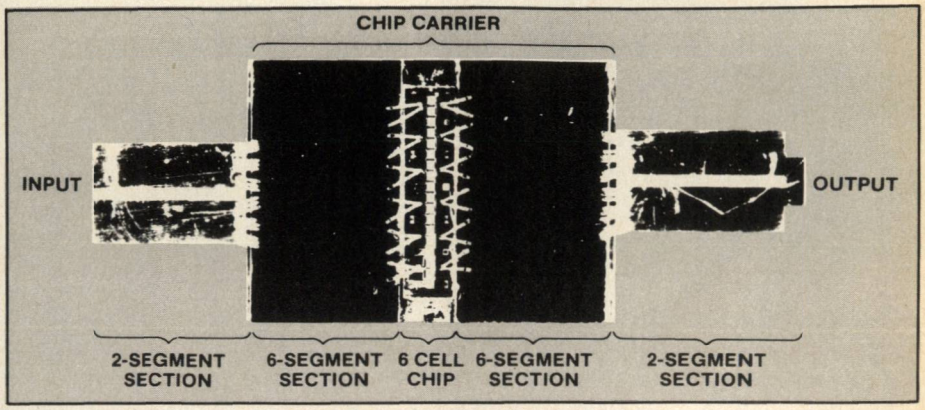

Fig. 7 FET amplifier/combiner circuit.

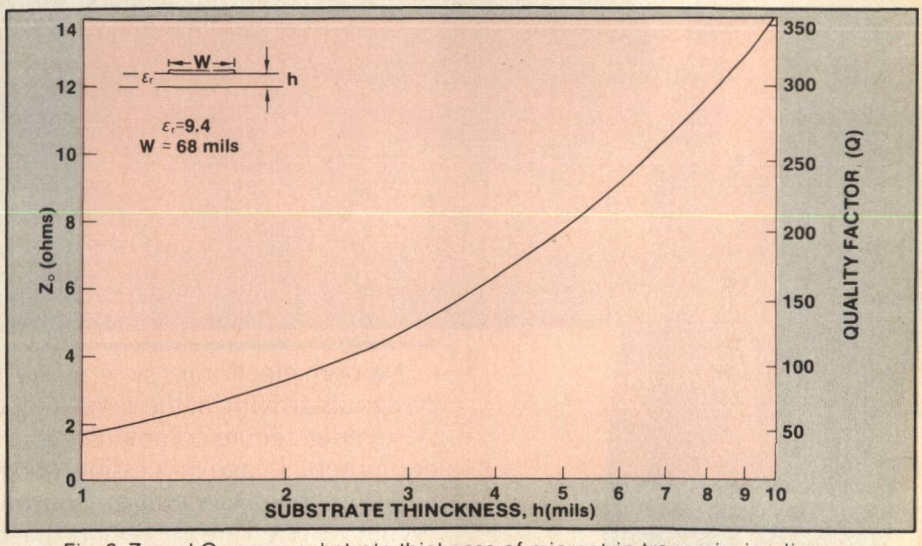

Fig. 8 Z_o and Q versus substrate thickness of microstrip transmission lines.

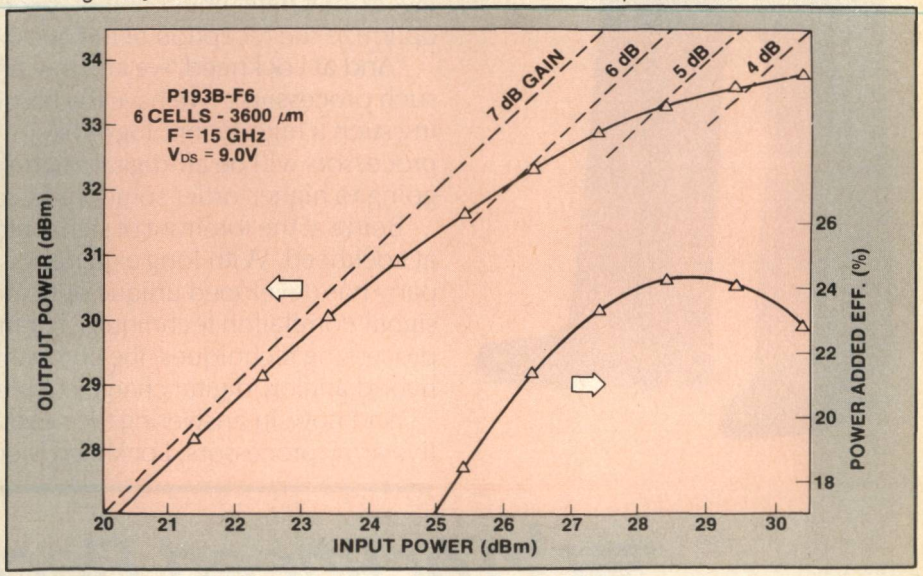

Fig. 9 Performance of FET combiner at 15 GHz.

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TABLE 1
SUMMARY OF FET CELL COMBINER PERFORMANCE

Device No.	Frequency (GHz)	Output Power (Watts)	Associated Gain (dB)	Linear Gain (dB)	Efficiency η_{pa}(%)
P109 (1cell)*	15	0.45	4.9	7.0	31
P142 (2 cell)	15	0.81	4.5	6.2	26.5
P109 (5 cell)	15	1.68	3.9	5.6	26
P193B (6 cell)	15	2.3	4.2	6.8	24.1
P204 (6 cell)	15	2.2	4.1	7.1	25.5
P209 (6 cell)	15	2.1	4.9	6.2	27.9
P100 (6 cell)	15	2.0	3.9	5.7	27.5
P100 (6 cell)	16	1.83	3.8	5.4	24.9
P100 (6 cell)	17	1.54	3.9	5.0	20.6
P100 (6 cell)	18	1.25	3.5	4.5	16.3

*Single cell device - no combiner circuit

lumped element circuits used for matching power FETs have a Q of only 40-50.

RF Performance

The performance of one of the best 6-cell chip-level combiners is illustrated in Figure 9. The device produced an output power of 2.3 watts at 15 GHz with an associated gain of 4.2 dB and a power added efficiency of 24.1%. This represents a power density of 0.64 watt/mm at 15 GHz. While this performance was obtained with the aid of tuning on the output circuit, the combiner as shown in Figure 7 is nominally matched to 50Ω. The small-signal gain of an untuned 6-cell combiner is shown in Figure 10. As illustrated in the figure, the 1-dB bandwidth is 1.7 GHz with a maximum gain of 4.5 dB at 16.6 GHz.

The performance of a 2-cell and a 5-cell version of the combiner together with several 6-cell combiner results is summarized in Table 1. The best single cell result is also included in the table for reference. All of the 6-cell combiners produced an output power of at least 2 watts at 15 GHz and a power added efficiency ranging from 24.1 to 27.9%. The 5- and 2-cell versions performed equally well with a corresponding reduction in output power.

In addition to the 15 GHz measurements, device P100 was evaluated at 16, 17 and 18 GHz and its performance is also summarized

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in Table 1. It is significant to note that with the exception of the single cell device, this performance data is amplifier level and not device level data. Circuit losses are included in the measurements. This data represents new state-of-the-art performance levels. The high efficiency, in particular, is significant. Drain efficiencies in excess of 45% are frequently observed at 15 GHz with the devices mounted in combiner circuits.

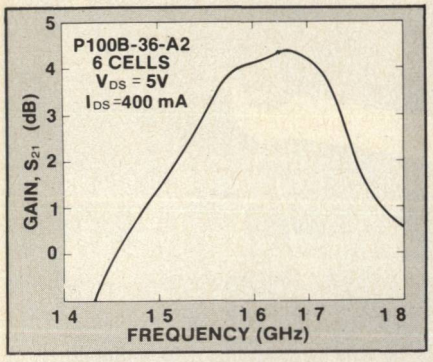

Fig. 10 Frequency response of untuned combiner.

Conclusion

A new planar power combiner, suitable for FET cell combining at frequencies ranging from 10 to 30 GHz, has been demonstrated. This new combining technique, as a 6-way chip-level combiner, has established new state-of-the-art performance levels for power FETs at Ku-band frequencies. It has demonstrated both high efficiency and moderate bandwidth capability. The key element of this approach is the application of circuit-level power combining concepts to the problem of chip-level cell combining, and the resulting development of the planar combiner. This planar combiner makes it possible to obtain high cell combining efficiency (>90%) at Ku-band and higher frequencies where other techniques fail.

Acknowledgements

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GaAs Impatt Diodes For Satellite Communications

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Introduction

Because the frequency bands below 14 GHz allocated to satellite communications are becoming crowded, the next generation of systems will use yet higher frequencies extending upwards into the millimeter-wave bands. Traditionally, the transmitters, both in the satellites themselves and in the earth stations, have been powered by TWT amplifiers. At higher frequencies, smaller, higher-gain antennas can be used, so that only moderate power levels are required. Since at present EHF TWTs have a limited lifetime (about 5000 hours) and also require sometimes impractical high-voltage power supplies, solid-state power sources are an attractive alternative.

Over the past decade significant advancements in the properties of solid-state devices have been achieved, and they are now seriously challenging the microwave tubes in the low and medium ranges. Principal advantages of these devices are: small size, low voltage power supply requirements, and potentially higher reliability than tubes. However, this last advan-tage has yet to be demonstrated in the field.

This work was supported in part by the Air Force under contracts F33615-77-C-1186 and F33615-80-C-1075.

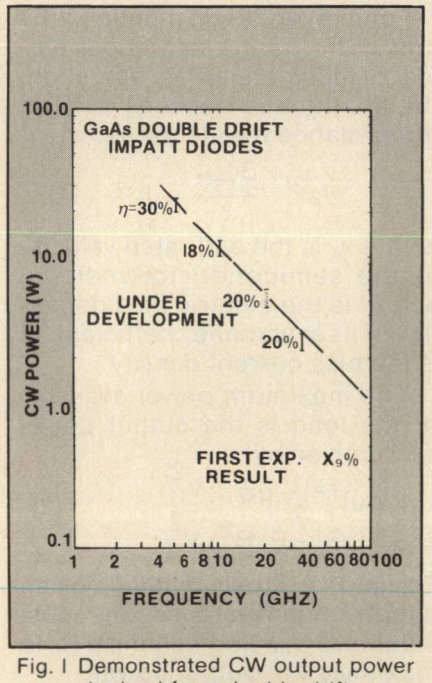

Fig. I Demonstrated CW output power obtained from double-drift, double-Read GaAs IMPATT diodes. (The conversion efficiency is shown.)

In terms of CW power and efficiency, IMPATT diodes outrank all other solid-state devices at frequencies greater than 20 GHz. They are also noisier, but when used in the final stages of a power amplifier this should not be a problem.

Silicon (Si), gallium arsenide (GaAs), and indium phosphide (InP) are all being considered as material for IMPATT diodes operating above 20 GHz. Based on our analysis and experimental results, we believe that for CW power sources GaAs will prove to be the best material.

We have developed GaAs IMPATT diodes using double-drift, double-Read material with properties optimized to give maximum power output and conversion efficiences at the required frequencies. Figure 1 shows the best results obtained in the laboratory at each frequency for our IMPATT devices operating as free-running oscillators.

The 20 GHz diode is now under development, and we have achieved 4 W CW at 20 percent efficiency, close to our goal of 6 W. In the 35 to 45 GHz range, power outputs greater than 2 W are obtained fairly routinely, the best one being 3 W at 22 percent, efficiency measured at 34 GHz. An initial result was obtained at 55 GHz using non-optimized material and circuit. We measured 400 mW of power with 9 percent conversion efficiency.

The outstanding performances obtained with GaAs IMPATT diodes have been the result of advances in the state of the art of material growth and device fabrication and packaging, as well as a better understanding of the diode physics through the use of large-signal characterization and modeling. Further improvements in device reliability are also pursued actively.

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The IMPATT Diode

The simplest representation of an IMPATT diode is given by the schematic of Figure 2. It is the parallel combination of a negative conductance G and a capacitive susceptance B; in a series with this combination is a resistance R_s which represents all the losses in the diode chip, the package, and the impedance transformers, all referred to the plane of the diode.

The circuit, which includes the package parasitic reactance, the transformer and coupling structures, and the load, is assumed to consist of a resonating inductance L and a load g_φ. The magnitude of the diode admittance Y(Y=G+jB) is a function of dc bias, junction area, material parameters, and RF voltage amplitude V_{RF}.

For a given diode junction area and at RF voltage amplitudes typical of millimeter-wave operation, the admittance depends only on the avalance frequency ω_a.

$$\omega_a^2 = \frac{3v_s\alpha'}{\varepsilon} \cdot J \qquad (1)$$

where v_s is the saturated velocity in the semiconductor material and α' is the electric field derivative of its avalanche coefficient.[2] J is the bias current density.

The maximum power available at the load is the output power and is given by

$$P_{out} \approx \frac{1}{2} g_\varphi \cdot V_{rf}^2 = \frac{1}{2} (|G| - R_s B^2) V_{rf}^2 \qquad (2)$$

Equation 2 shows that for a given negative conductance, one must maximize V_{RF} and minimize R_s to maximize the output power.

Compared with silicon and InP, GaAs has the highest mean mobility of electrons and holes, so that it will show the lowest series resistance. We believe that a significant portion of the series resistance occurring in millimeterwave diodes comes from the semiconductor regions which are undepleted during at least a portion of the RF cycle, as well as from buffer, substrates, and contact layers. It has been argued that InP has a higher saturated velocity than GaAs with an associated longer optimum drift zone, resulting in a performance advantage at millimeter wave frequencies due to a proportionately larger V_{RF}. An efficiency advantage for InP has so far not been demonstrated, most likely because at a given input dc power |G| is much smaller in InP.

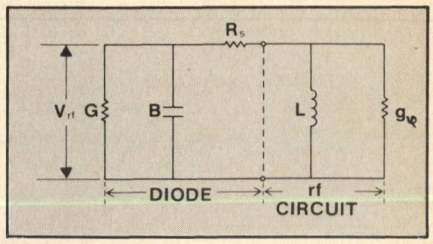

Fig. 2 IMPATT diode equivalent circuit.

The primary reasons for the smaller negative conductance are the associated lower bias current density due to the higher dc bias voltage and the apparently smaller value of α' in InP.[3,4] These points, taken together with observed high values of electrical series resistance in InP,[5] may explain why so few results are available from InP IMPATT diodes operating in the CW mode.

Compared with silicon, GaAs has the advantage of using a Read structure with a low-high-low doped avalanche zone. Such structures, which have never been practically implemented in silicon, lead to higher efficiencies because the maximum RF voltage amplitude relative to the operating voltage is higher in a diode with a well-defined avalanche zone than in one where the avalanche zone can spread into the drift region of the diode.

In view of the considerations given above, we have selected GaAs as the material having so far the greatest potential for high-frequency applications. The IMPATT diodes developed in our laboratory are all double-drift, double-Read structures made of GaAs.

Diode Fabrication

A typical double-drift, double-Read semiconductor material doping profile is shown in Figure 3. Note the large variations of doping levels to be realized within very small spatial dimensions. At frequencies below 40 GHz, adequate doping control can be obtained from vapor-phase epitaxial growth (VPE) but at the higher

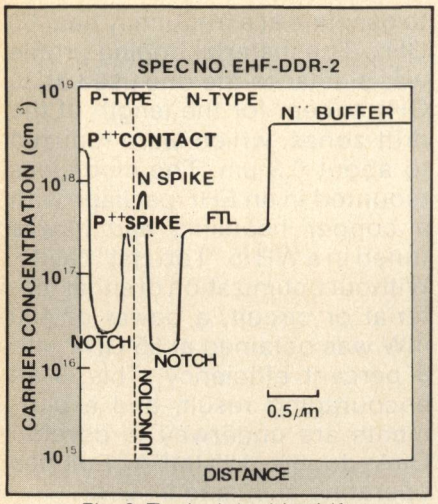

Fig. 3 Typical double-drift, double-Read profile. (dimension shown for 35 GHz.)

frequencies we are using alternative methods which permit lower growth rates, for instance, molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), and low-temperature VPE. Each epitaxial layer is grown sequentially on top of a conductive substrate without removing the wafer from the reactor. The n-side of the diode is usually doped with silicon, the p-side with zinc. Great care is exercised to have a p-n junction as abrupt as possible and to minimize the spacing between the two spikes of charges. After growth, each wafer is carefully characterized by measuring its doping profile, and those meeting predetermined specifications are further processed into diode chips.

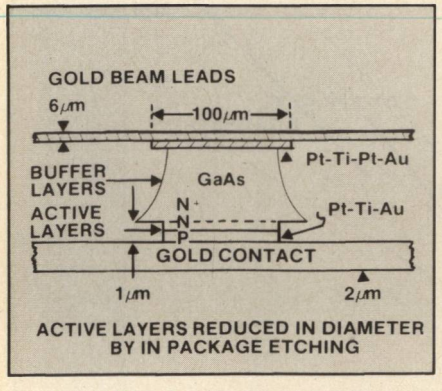

Fig. 4 Diode mesa cross section.

Figure 4 shows the cross section of a typical 40 GHz diode mesa. The general features of these diodes are:

- mesa height of 8 to 10μm,
- mesa diameters of 100 μm,
- plated gold contact thickness of 2μm, and
- four gold beam leads plated directly to the top contact of the mesa.

The short mesa height permits the series resistance from contact and buffer layers to be kept small and minimizes the under-cutting of the top contact upon etching the small 100 μm diameter mesa. The thin gold contact permits thermal-compression bonding of the chip directly to a diamond without solder and without a thick metal layer which adds unwanted thermal resistance.

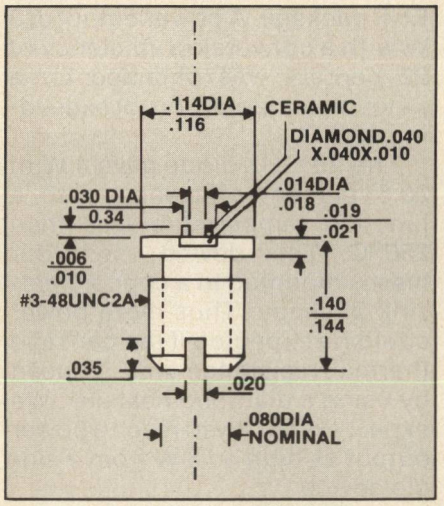

Fig. 5 Typical EHF diode package with diamond heatsink.

The gold beam leads are essential for making reproducible and reliable diodes of the small dimensions required at 40 GHz and above. These leads obviate the need of seperate wires which must placed by hand. Such wires are usually not reproducible in length or shape. They require a separate bonding operation which adds unnecessary mechanical stress to the mesa.

The diode chips are mounted in specially designed packages to reduce thermal impedance and parasitic reactances. This package is shown schematically in Figure 5. It is threaded so it can be easily mounted and removed from test fixtures. The junction temperature rise of a diode is given by:

$$\Delta T = \theta \cdot P_{out} \left(\frac{1}{\eta} - 1\right)$$

[Continued on page 74]

[From page 73] **GaAs**

To maintain ΔT at reasonable levels as demanded by the device reliability requirements, θ, the thermal impedance of the diode, must be reduced to a minimum. We make use of the very high thermal conductivity of the diamond to achieve this goal. A ceramic ring is attached on top of the diamond to form an enclosure for the diode chip.

Diode Performance

The best output power measured on our diodes at the present time is shown in Figure 6. The 34 GHz diode has a single mesa mounted in a diamond heat-sink EHF package. A power output of 3 W with a conversion efficiency of 22 percent was obtained for a junction temperature not exceeding 260° C.

The 20 GHz diode gave 4 W at 20.5 percent efficiency, with a junction temperature less than 250°C. This device used four mesas mounted in a copper heatsink package. Thus more power could be expected if the package thermal resistance was reduced by using a diamond heatsink. We expect eventually to reach a power output as high as 8 W from a single device.

A preliminary set of measurements was taken on a diode made to oscillate at a frequency near 60 GHz. The material doping profile was similar to the one used at 35 GHz except for the length of the drift zones, which were reduced to about 0.3 μm. The diode was mounted in an EHF package with a copper heatsink, and it was tuned in a WR 15 "Top Hat" cavity. Without optimization of either material or circuit, a power of 400 mW was obtained at 55 GHz with 9 percent efficiency. This is an encouraging result, and experiments are underway to develop GaAs double-drift IMPATT diodes operating at 60 and 94 GHz.

It is well known that the negative conductance of IMPATT diodes is a slowly varying function of frequency. Thus wide band operation is available in an appropriate circuit. Figure 7 shows the power output of one diode measured as a function of frequency for two different bias currents. The diode junction temperature rise is indicated for each operating point. The circuit was retuned for maximum power output in each case. In the figure we also show the results of calculations made using our large-signal diode model. The RF voltage was evaluated from our measurements of negative conductance and the measured series parasitic resis-

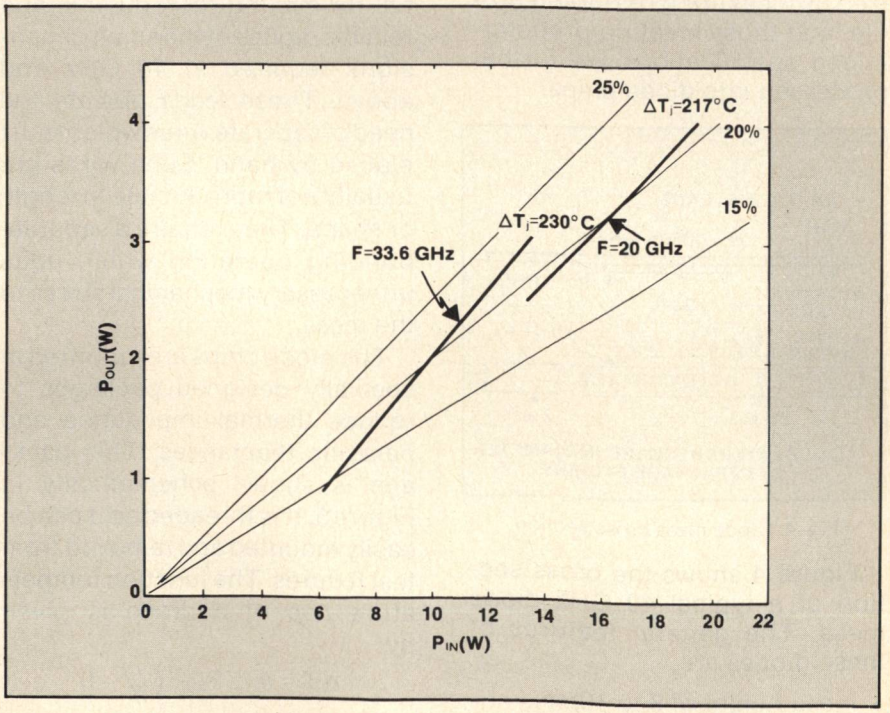

Fig. 6 P_{out} vs P_{in} for two GaAs IMPATT diodes.

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[From page 74] **GaAs**

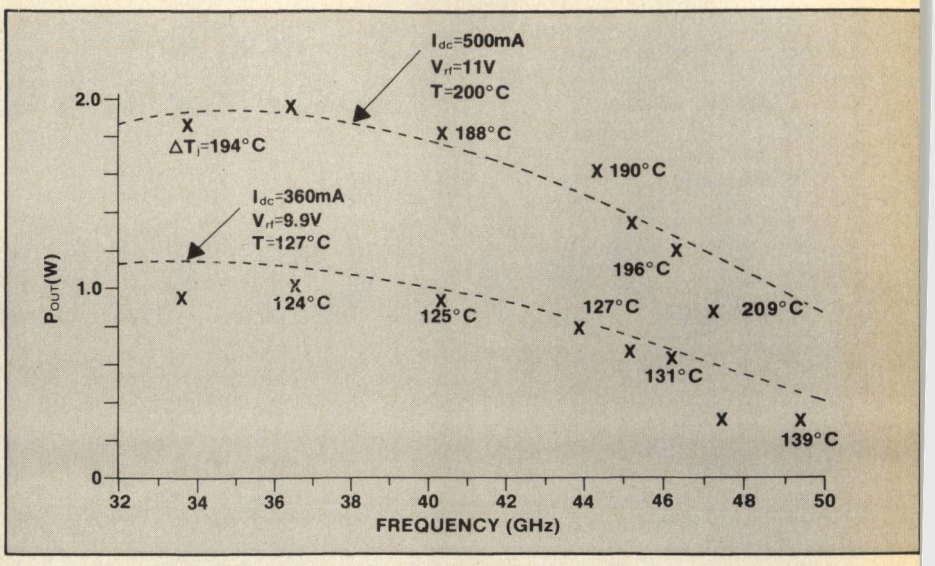

Fig. 7 Output power vs frequency for an EHF diode with diamond heatsink.

tance (R_s = 0.39Ω). The agreement between the calculations and the measurements is very good.

The oscillator power changes less than 3 dB from 32 to 50 GHz. Of course, the instantaneous bandwidth of a diode operating as an amplifier in a fixed tuned circuit would be less than this, but with an appropriate circuit design, a usable bandwidth of 6 to 10 percent can be achieved as shown in Figure 8.

A stable amplifier was built with one 35 GHz IMPATT diode. It gave a 10 percent bandwidth with a gain of 5 to 6 dB. The diode used has a copper heatsink and supplied 1.3 W at 35 GHz as an oscillator. The saturated power output of the single-stage amplifier varies between 0.6 and 1.0 W. By using the same diode in an injection-locked oscillator, we could have reached a power output near that of the free-running oscillator but with a much narrower bandwidth.

Reliability

Since the reliability of a solid-state transmitter depends almost solely on the active device used, it is extremely important to be able to evaluate the mean time to failure (MTTF) of the IMPATT diodes. An MTTF of up to ten years (10^5 hours) is often required for solid-state components used in communcations. Such long operating lifetimes can be measured only through accelerated stress life testing. The technique applies operating conditions qualitatively similar to those encountered in actual field service to a population of devices, but the stress level (usually the diode operating junction temperature) is increased to induce failures within a relatively short interval. Then, lifetime under ordinary operating conditions is projected from statistical analysis of the failure data obtained under high-stress conditions.

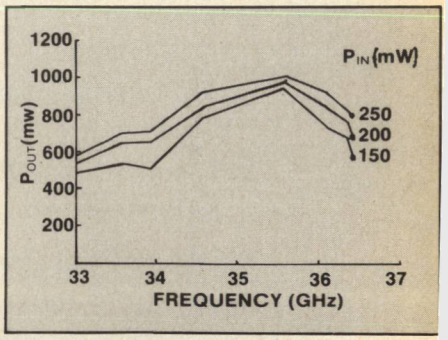

Fig. 8 Frequency response of a single-diode stable amplifier stage.

The life test of IMPATT diodes under large RF signal conditions is prohibitively expensive for the number of diodes that constitute a statistically acceptable population. One must, in general, be content with a small sample of devices in an RF test along with a larger sample in an alternative (but less expensive) dc test.

In the technique we use, the junction temperature is adjusted by varying the input dc power applied to the diodes. The stresses produced by thermal gradient and by the increased current flow are greater than normally encountered and most likely produce pessimistic results, but it is the method

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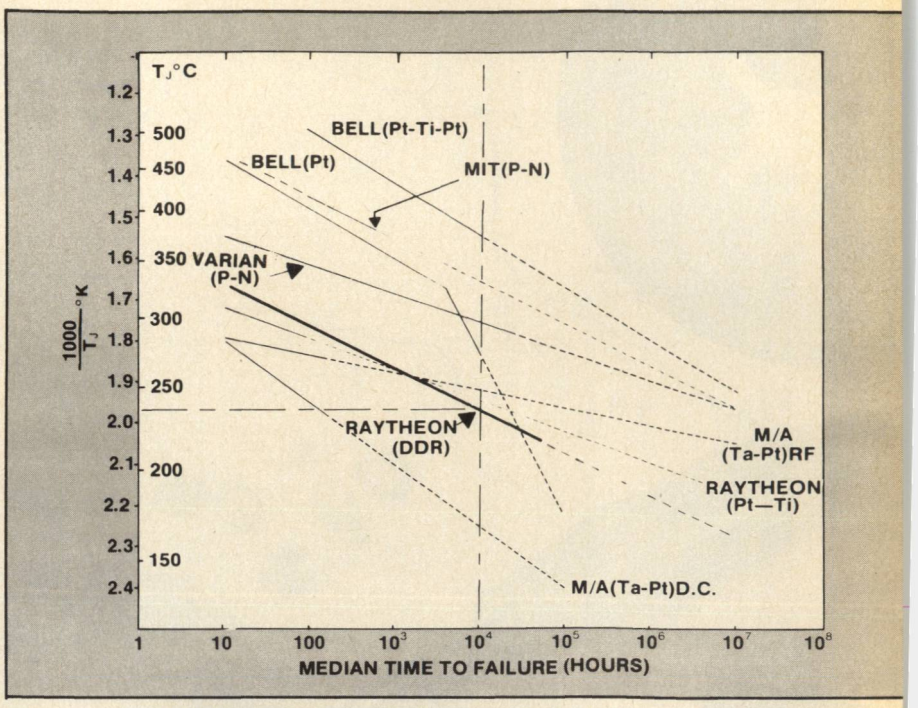

Fig. 9 Published reliability data for GaAs IMPATT diodes.

most commonly used.

Figure 9 shows some of the published reliability data for GaAs diodes, collected and plotted on a common scale. The solid lines indicate the range of conditions for tests actually performed. Dashed lines represent extrapolations based on the assumptions that failures are thermally activated according to the Arrhenius law. The plotted data varies widely, probably because different diode structures with different metallization systems were subjected to different kinds of thermal and electrical stresses and therefore failures were judged by different criteria. In addition, the sample sizes are often small and the statistics consequently unreliable.

The curve for the Raytheon double-drift Read diodes (DDR) was obtained for diodes with a AuGe alloyed contact on the n^{++} doped buffer layer. This contact was later shown to cause failure of the diode because of gold-gallium migration. By changing the metallization system to use a diffusion barrier (Pt,Ti,Pt), the MTTF has been increased by an order of magnitude for a given junction temperature.

Conclusion

Gallium arsenide double-drift IMPATT diodes can be used as the active element in satellite communications transmitters operating at frequencies above 14 GHz. High power and conversion efficiencies have been obtained at 20, 35, and 44 GHz, and we have demonstrated promising results showing these devices to be useful at yet higher frequencies. Continuing progress in the processing and packaging technologies should result in devices sufficiently reliable to meet the rigid requirements demanded by their use in practical communication systems.

Acknowledgement

The authors wish to express their appreciation to their many colleagues in the Semiconductor Laboratory at Raytheon Research Division for their vital contributions to this work.

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Beam Lead IMPATTs - A New Dimension

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Introduction

Like the most other semiconductor devices, the packaging aspects of IMPATT diodes also become more critical as the frequency increases. For millimeter wave IMPATT diodes operating in the frequency range of 30 to 300 GHz, the packaging techniques and package parasatics reduce the available output power and efficiency, decrease reliability and provide a significant variation in the package parameters from device to device. All these factors also reflect on the device manufacturability. Since IMPATT diodes are the only viable source of high power millimeter wave energy using solid state devices, the growing future of millimeter wave systems warrants a critical look at their packaging technology. The beam lead technology reported here adds a new dimension to the millimeter wave IMPATT diode manufacturability by contributing to the device technology areas mentioned above.

The beam lead per se is an old concept and has been the backbone of hybrid circuits and various microwave integrated circuit approaches for about a decade. What is new in this technology is the three-dimensional beam lead structure. Thus, unlike the conventional beam lead devices where all the electrical connections are brought out in one plane, the three-dimensional beam lead IMPATT diode has only one terminal available via beams and the other terminal is on the bottom side of the semiconductor chip. Thus, whereas the conventional beam lead devices are used directly into the circuits, the beam lead IMPATTs are packaged prior to their use in the circuits. The direct use of unpackaged beam lead IMPATT, in microwave and millimeter wave integrated circuits will soon emerge.

This paper describes the technology being developed for 94GHz pulsed silicon IMPATT diodes in the three-dimensional beam lead configuration. Although the technology is being developed for IMPATT diodes, it will open new avenues for other device types for integration in the microstrip and dielectric waveguide (including image and insular guide) circuits at microwave and millimeter wave frequencies.

Beam Leads and IMPATT Diodes

In the conventional beam lead devices, after the semiconductor device structure is fabricated and before the individual devices are separated from the starting wafer, the cantilever beams are formed using such processes as metallization, photolithography — electroplating, etc. This leads to such advantages as uniformity of lead dimensions, elimination of the need for bonding leads on to the semiconductor chip, realization of a self-contained package eliminating the need of an external package and reducing the overall size, ease and compactness of device integration in the circuits, etc. This conventional beam lead technology, however, has been adopted only to those devices which can be realized in planar configuration without significantly affecting the performance. For high power IMPATT diodes, how-

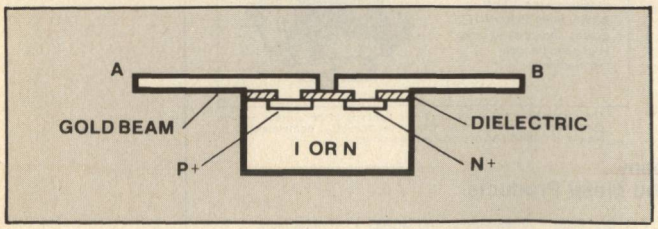

Fig. 1 A conventional beam lead diode structure with two diode terminals in one plane.

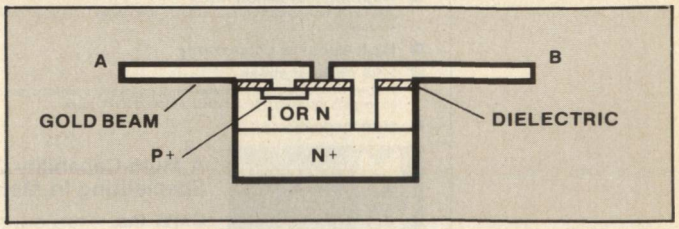

Fig. 2 A vertical beam lead diode structure with two diode terminals in one plane.

ever, for reasons of heat sinking and mesa construction requirement, such a beam lead process has not previously been adopted.

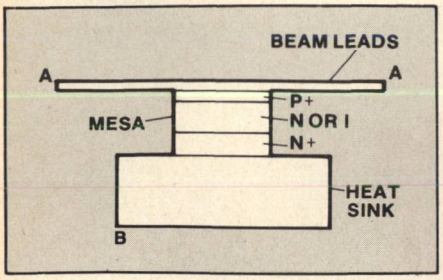

Fig. 3 A three-dimensional beam lead diode structure with one diode terminal as beams and the other on the bottom of the mesa as heatsink.

In order to improve the uniformity of package parasitics in general and lead inductance in particular, use of prefabricated beams or bow ties and beam leads instead of wires or ribbons has been attempted. These prefabricated beams significantly improve the device uniformity and reproducibility. This approach, however, does not solve another major problem of bonding the prefabricated beams on the top of the mesa. In this bonding process, since the mesa dimensions are generally smaller than the prefabricated beams and much smaller than the bonding tool, it leads to such conditions as chipping and microcracks and ultimately reflecting on device yield through packaging and on long term reliability. This problem is solved using the three dimensional beam-lead structure described here.

Three-Dimensional Beam Lead Structure

Figure 1 shows a conventional beam lead diode structure and features the two beam lead terminals of the diode in the same plane. As an extension of this technology, Alpha has developed a vertical beam lead diode shown in Figure 2 and more recently a mesa beam lead diode. These two structures also have the two beam leaded diode terminals in the same plane. In contrast to these structures, a three-dimensional diode structure shown in Figure 3 is the key to the practical beam lead IMPATT diodes, especially at millimeter wave frequencies. This structure features 2 or 4 beams, photo lithographically realized on the top of the diode mesa and thus all the beams represent the same terminal of the diode. The other diode terminal is on the bottom side of the mesa and is accessible as the plated heatsink. Besides the uniformity of the lead dimensions, and the corresponding electrical parameters, this three-dimensional beam lead structure eliminates the need of bonding an electrical connection onto the top of the mesa and hence improving device yield. The elimination of bonding on the top of the mesa also eliminates the problem of microcracks in the mesas.

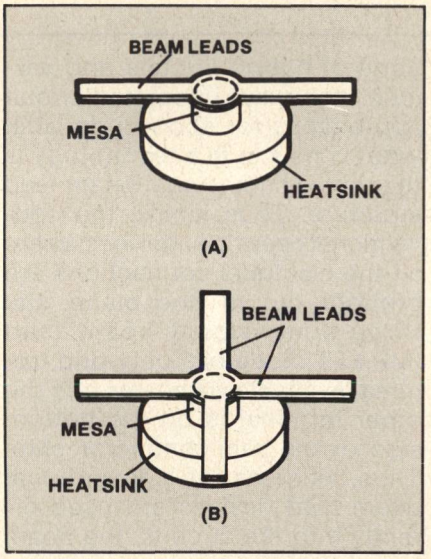

Fig. 4 Configurations for three-dimensional beam lead millimeter wave IMPATT diodes.

Beam Lead IMPATT Fabrication

Although the feasibility of 4-beam diode structures such as shown in Figure 4 has been demonstrated in the past, the essential process steps developed to date for realizing this structure are shown in Figure 5. The conventional IMPATT fabrication steps required prior to the first stage shown in Figure 5 are not included here. These steps include epitaxy for active layer on a low resistivity substrate, single or double drift structure formation using ion implantation, diffusion, etc., metallization for front ohmic contact, heatsink plating, sub-

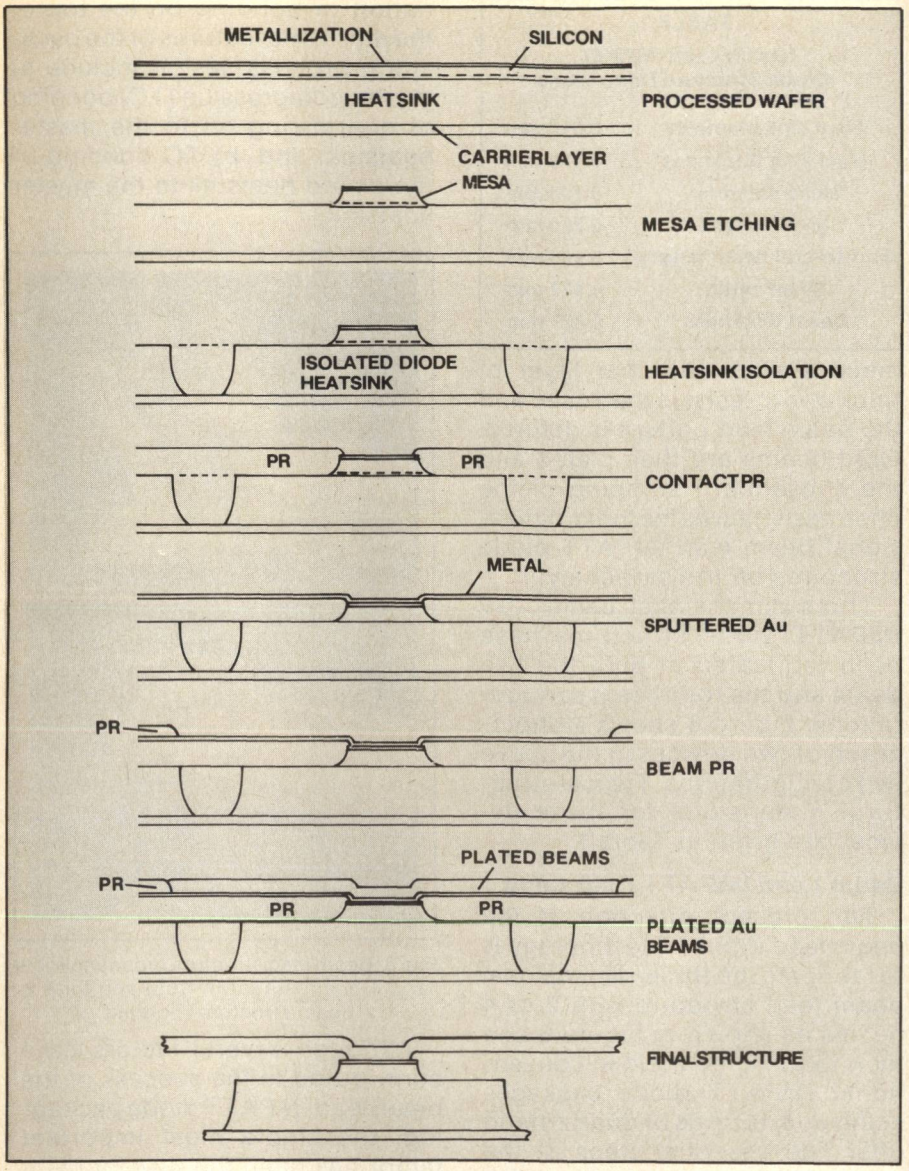

Fig. 5 Three dimensional beam lead IMPATT diode fabrication process.

strate thinning and back metal realization. The metallization identified in Figure 5 is the back or top metallization.

Fig. 6a A 2-beam W-band beam lead IMPATT diode.

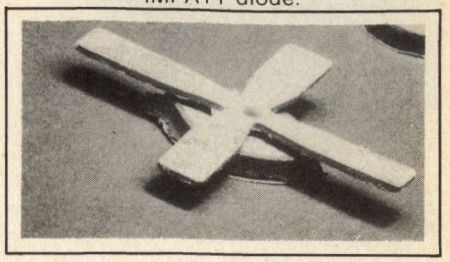

Fig. 6b A 4-beam W-band beam lead IMPATT diode.

For developing the 94GHz beam lead IMPATT diode technology, single drift structures in n-type silicon have been used as a vehicle. After realizing the device vertical structure, silicon mesas are defined and etched. The heatsinks for the individual diodes are then defined and isolated. A 1 mil thick rigid photoresist is then used and beam lead contact areas are opened in the photoresist on the top of the mesas. After cleaning the opened contact area including an ion milling step, the wafer is metallized with a multilayer

[Continued on page 84]

[*From page 83*] **IMPATTS**

TABLE 1
Beam Lead IMPATT Diode Structure Dimensions

Heat sink diameter	0.510 mm
Heat sink thickness	0.076 mm
Mesa diameter	0.100 mm
Mesa height	0.010 mm
End-to-end beam length	0.890 mm
Beam width	0.127 mm
Beam thickness	0.025 mm

metal system. Another layer of thick photoresist is then used and the beam lead pattern is defined. Gold beams are then plated and the subsequent stripping of the photoresist leaves the three-dimensional beam lead IMPATT diode structures on the carrier layer.

Three-dimensional beam lead IMPATT diode structures have been fabricated in both the two beam and the four beam configurations. Figure 6 shows a photograph of two devices in the above two configurations. Typical structural dimensions for these devices are given in Table 1.

Beam Lead IMPATT Packaging

The present direction of the beam lead IMPATT technology is to fabricate the three-dimensional beam lead structure with 2 or 4 beams as shown in Figure 6 and then to package them in conventional IMPATT diode packages using quartz rings or quartz stand offs. The essential steps of the packaging process are shown in Figure 7. In addition to the elimination of bonding on the top of the mesa, the features of the packaging process design include a) thermocompression (TC) bonding of quartz ring on to the master heatsink, and, b) TC bonding of the plated heatsink to the master heatsink.

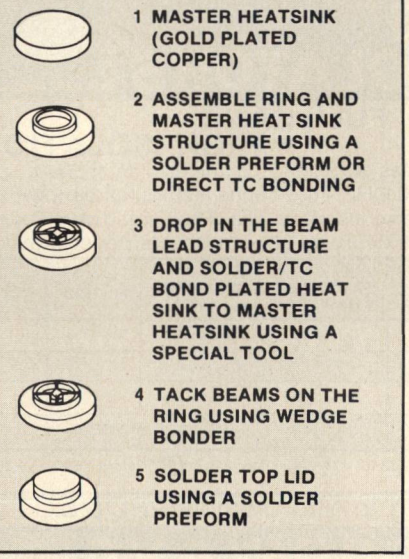

Fig. 7 W-band beam lead IMPATT diode assembly process design.

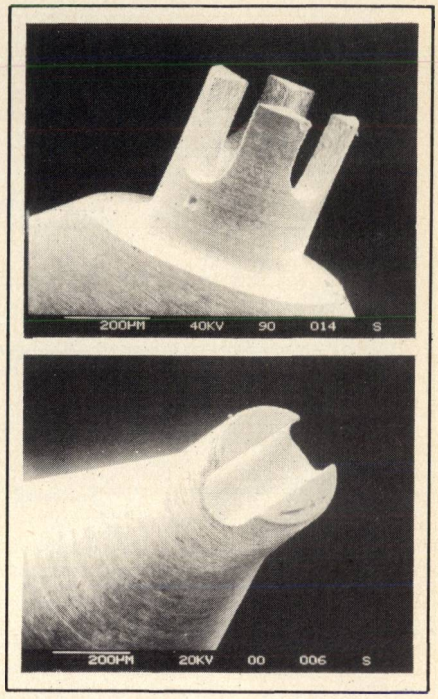

Fig. 8 Beam lead structure mounting tools for a 4-beam structure (top) and for a 2-beam structure (bottom).

Although several factors have contributed to the success of the beam lead IMPATT diode packaging, the single most important factor has been the development of special tools for thermocompression bonding of the diode heatsink on to the master heatsink inside the quartz ring. These special bonding tools have been developed for both the two and four beam configuration. Figure 8 shows photographs of these two special tools. In these tools, the prongs of the tool go around the beams and transmit the pressure on the top of the plated heatsink as required for thermocompression bonding. Figure 9 shows the photograph of a packaged beam lead IMPATT diode.

Test Results

Single drift silicon beam lead IMPATT diodes fabricated and packaged as described above, have been evaluated for their RF performance capability in a full height, electroformed, W-band

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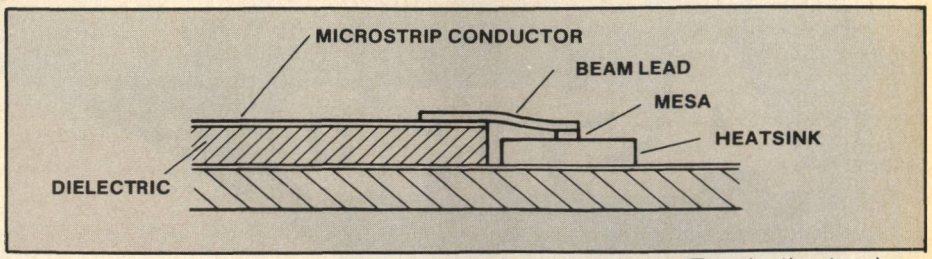

Fig. 10a One beam diode configuration for microstrip circuits (Termination type).

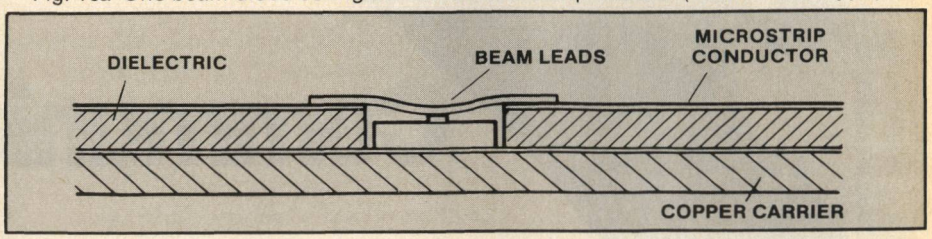

Fig. 10b Two beam diode configuration for microstrip circuits (Transmission type).

waveguide circuit with built-in E-H tuner close to the diode plane. Pulse output power of up to 3.5w at about 94GHz has been achieved with a pulsewidth of about 100ns and a pulse repetition rate of 40 kHz. This represents the highest output power reported from the single drift IMPATT diodes in this frequency range.

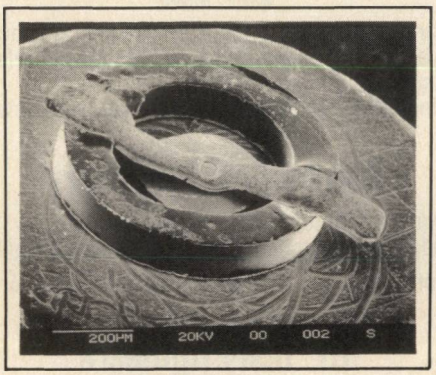

Fig. 9 Packaged W-band beam lead IMPATT diode without cover.

Future Promise of The Technology

The three-dimensional beam lead structure has made a significant contribution in the millimeter wave IMPATT diode technology. State-of-the-art results have been obtained using packaged single drift devices. The basic unpackaged three-dimensional beam lead IMPATTs will open new avenues for active device integration in the millimeter wave integrated circuits. This device geometry is very suitable for integration into such circuit media as microstrip, stripline, image guide, insular guide, etc. The bonding tools developed will be the key to the future success. Some specific potential growth areas are as follows:

- In microstrip circuits, the beam lead IMPATT diodes can be easily mounted across the transmission line. Thus, the two possible configurations using one beam and two beam structures are shown in Figure 10. Both these configurations are suitable for amplifier and oscillator application.
- The configuration of Figure 10 when used for three-dimensional beam lead PIN diodes will add a new dimension to the PIN diode circuit technology — by making it possible to incorporate shunt PIN diodes in transmission lines with low parasitics.
- The thin substrate technology of IMPATT diodes in conjunction with the three-dimensional beam lead structure will lead to mechanically rigid, small area, low parasitic PIN diodes, suitable for fast millimeter wave switching and phaseshifting applications, with relatively high power handling capability.

Acknowledgments

The author acknowledges the contributions of Mr. Gene Baker in the development of the beam lead technology with technical support from M/S Cal Watts, Kurt Irlesberger, Bob Balance and Ms. Sarah Lambert. The beam lead technology work was done under contract no. DAAK20-80-C-0308, U.S. Army ERADCOM, Electronics Technology and Devices Laboratory. ■

Broadband Monolithic MIC Power Amplifier Development

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Introduction

The future production of low cost GaAs monolithic amplifiers is dependent upon the development of key fabrication technologies and circuit design techniques which not only promote low cost, but do not degrade the electrical performance of the monolithic devices. In keeping with this theme, this article presents a brief discussion of the fabrication technologies being used at Westinghouse along with a more detailed presentation of the circuit design, optimization and experimental measurements performed on a two stage, 5-10 GHz, 1 W monolithic amplifier. A 3 W, 8-12 GHz, four stage monolithic amplifier is currently under development which presents special design problems because of the large periphery FET required in the output stage. A design approach to this particular amplifier is also discussed.

The amplifer designs discussed herein are the outgrowth of a DARPA/NAVAIR sponsored program entitiled "GaAs Monolithic Subsystem Technology Base" which has been underway for approximately 3 years. This program has as its two main goals:

- the development of the technologies necessary for future low cost production of GaAs monolithic power amplifiers and,
- the development of broadband monolithic power amplifiers.

Early in the program, a commitment was made to a direct selective ion implantation (DSI^2) fabrication technology, since it was felt this offered significant cost advantages in a future production environment. In this approach, the active FET channels are formed by direct selective ion implantation into unbuffered, high purity LEC grown semi-insulating GaAs substrates[1,2]. This method eliminates the need for buffer layer growth and qualification, and subsequent mesa etching to define the active areas. The benefit of the high purity LEC grown substrates is evidenced by the fact that Si implants into theses substrates exhibit very high mobilities; i.e. for peak donor concentrations of $1x10^{17}$ cm^{-3}, mobilities of 4800 to 5100 cm^2/v-s are measured. One micron gatelength FETs fabricated using this DSI^2 approach typically exhibit 0.5-0.7 W/mm power output at 8 GHz.

The 1 micron gatelength photolithographic technology, while adequate for 5-10 GHz amplilfier designs, is being replaced by a deep UV technology in order to achieve 0.7 micron gatelength FETs with higher gain in the 8-12 GHz band.

Circuit Design

The main objective behind the development of GaAs monolithic amplifiers is to provide an inexpensive microwave amplifier on a chip. To the circuit designer, size is of primary importance in reducing amplifier cost. The smaller an amplifier can be made to perform a given function the more amplifier chips can be obtained from a given size wafer. For wideband amplifiers operating below 10 GHz, this desire to minimize overall chip size effectively precludes the commonly used balanced amplifier approach requires relatively large quadrature couplers on the input and output of each stage in addition to matched amplifier pairs.

In this paper, an alternate single-ended approach is described. This approach is based on load-pull characterization of the FET devices and has been used to design a two stage, 5-10 GHz monolithic amplifier with a power output approaching 1 watt.

One of the main questions which the power amplifier designer must answer is what impedances must be presented to the FET input and output terminals to produce maximum output power. Wideband

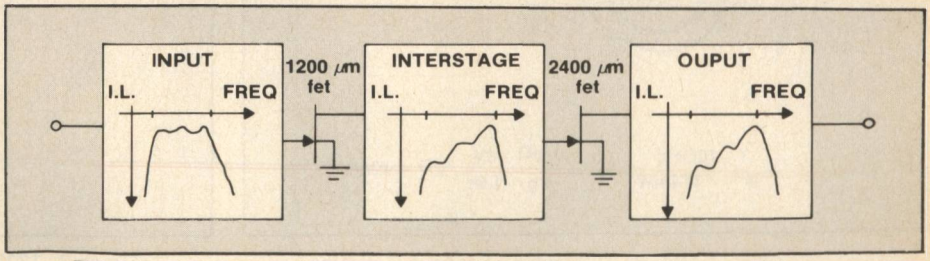

Fig. 1 Design approach to two stage 1W 5-10 GHz monolithic amplifiers.

amplifiers introduce the additional problem of requiring the 6 dB/octave/stage gain equalization necessary to compensate for the inherent gain rolloff of the FETs with frequency. For multistage amplifiers in general, the approach described here[3] consists of placing the full burden of gain equalization for each FET onto the circuitry immediately following that particular FET. This allows the input of the amplifier to be flatly matched across the band thereby retaining, at least to some degree, the good input match advantage of a balanced amplifier. Thus, for the two stage amplifier discussed in this paper and shown in Figure 1, the equalization for the 1200 μm first stage FET is provided by the interstage network. Flat drive power across the 5-10 GHz band is thereby obtained for the 2400 μm second stage FET. The 2400 μm FET is equalized by the output circuit thereby achieving flat power out of the amplifier as a whole across the design band. This process can be easily extended to more than two stages if desired.

In order to carry out the design approach described, it is necessary to obtain data indicating how the output power of each FET varies as a function of the load impedance presented to it. This information can be obtained, experimentally, through the use of the "load pull" concept.

For these measurements, an electronic load pull test setup[4] is used. With such a test setup any load impedance can be presented to the FET output under large signal conditions and the corresponding output power measured.

Therefore, a series of constant power contours for a fixed input power and bias point can be generated at each frequency of interest in the design band. Such a set of contours is shown in Figure 2 for the 1200 μm first stage FET at an input power of 174 mW at 10 GHz. The bias point for this FET is V_{DS}=8V, V_{GS}= -1.9V and I_D= 150 mA. At each frequency, there is only one load impedance which when presented to the FET results in maximum output power for a given input power. At 10 GHz, the 1200 μm FET has a maximum power output of 550 mW. This power level is particularly important since according to our design approach to gain equalization, the maximum output power at the highest frequency in the design band governs the output power of that stage across the band.

At 7 GHz the maximum output power has risen to 695 mW. The 550 mW level which was attainable by only one load impedance at 10 GHz is now attainable by a set of impedances lying on a locus shown at 7 GHz since the FET must be power mismatched to produce less than maximum output power.

The loci of impedances at 5 GHz producing the 550 mW level is even larger since the FET must be even more power mismatched.

The next step in the design procedure is to group together those contours which result in 550 mW output power into a set of composite contours as shown in Figure 3. The contours at 6, 8 and 9 GHz have also been included. Note that the composite contours are shifted more to the inductive end of the Smith chart than the individual frequency contours. This is due to the fact that the bondwires used to connect the FET to the test fixture have been accounted for since they obviously are not present in the monolithic amplifier. Note also that the composite contours represent not only constant output power, but also constant gain.

The function of the interstage network of providing gain equalization for the 1200 μm FET has become one of transforming the input impedance of the second stage 2400 μm FET composite contours at the corresponding frequencies. The input impedances to both the 1200 μm and 2400 μm FETs can be easily obtained from small signal measurements since it has been found that the input impedance of a FET does not vary appreciably with drive power.

A similar set of composite contours is generated for the 2400 μm FET at an input power of 348 mW as shown in Figure 4. This power level is slightly lower than the 550 mW which the first stage can deliver in order to compensate for interstage network losses. The function of the output network of pro-

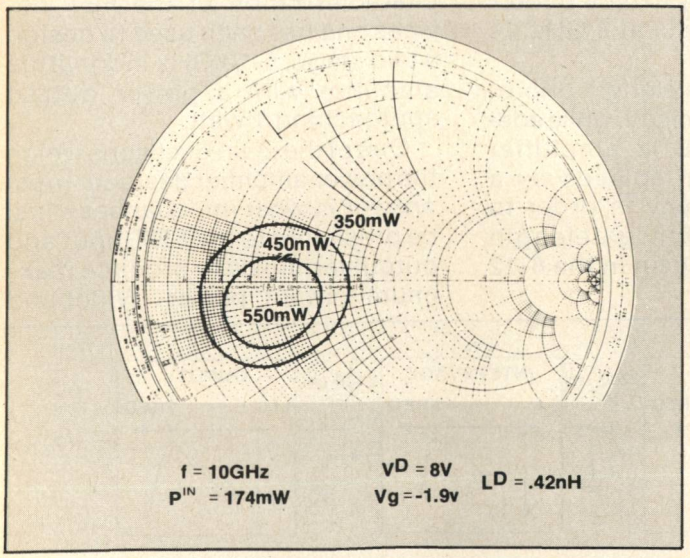

Fig. 2 10 GHz 1200 μm FET load pull circles.

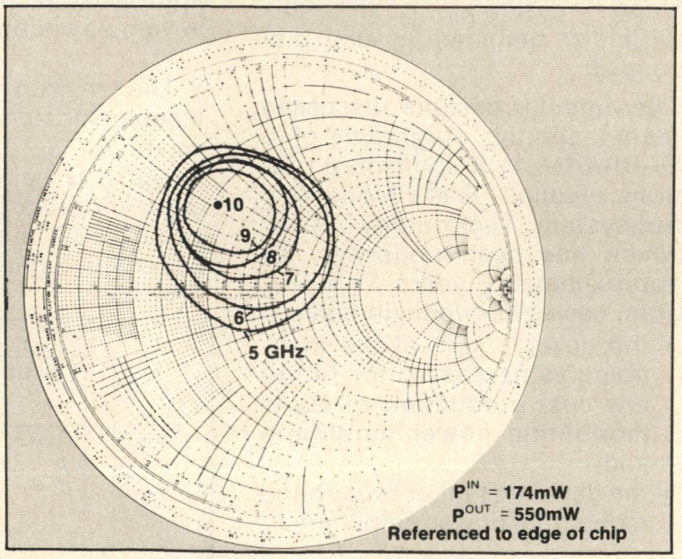

Figure 3. 1200 μm composite load pull contours.

viding gain equalization for the 2400 μm FET has become one of transforming the 50Ω load impedance to an impedance locus which crosses the 2400 μm FET composite contours at the corresponding frequencies. For example, Figure 5 also shows how the 50Ω load impedance is gradually transformed to the desired impedance locus by adding more and more circuit elements. Starting at the center of the Smith chart at 50Ω a series capacitor is added thereby moving along a constant resistance circle to the impedance locus shown at A. A shunt capacitor moves the impedance locus at A along constant conductance circles to the impedance locus shown at B. Next, a series inductor is added which moves the B impedance locus again along constant resistance circles to the impedance locus at C. Finally, adding a shunt inductor moves the impendance locus at C to the final approximate impedance locus at D. There are other paths which could have been taken on the Smith chart that would have resulted in an impedance locus which crosses the composite contours in such a manner as to give constant power out at each frequency.[5] However, the one chosen results in a circuit which is practical for biasing. By means of an off chip bypass capacitor, drain bias for the 2400 μm FET can be injected through the shunt inductor. DC blocking is then provided by the two output capacitors.

Once the basic circuit topology and initial circuit element values are obtained, the lumped inductors are replaced by short pieces of microstrip transmission line. Shunt parasitic capacitances associated with interdigital capacitors over a ground plane[6] are also added and the entire network is optimized using a special comput-

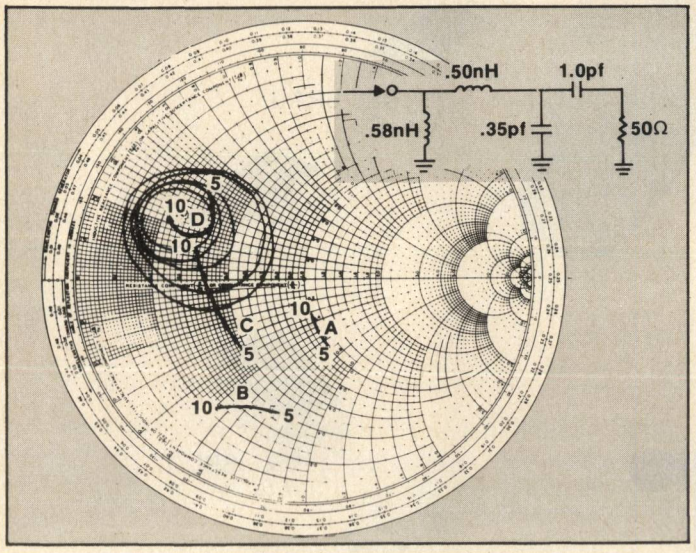

Fig. 4 2400 μm FET composite load pull contours. Impedance progression for the synthesis of the output circuit is shown.

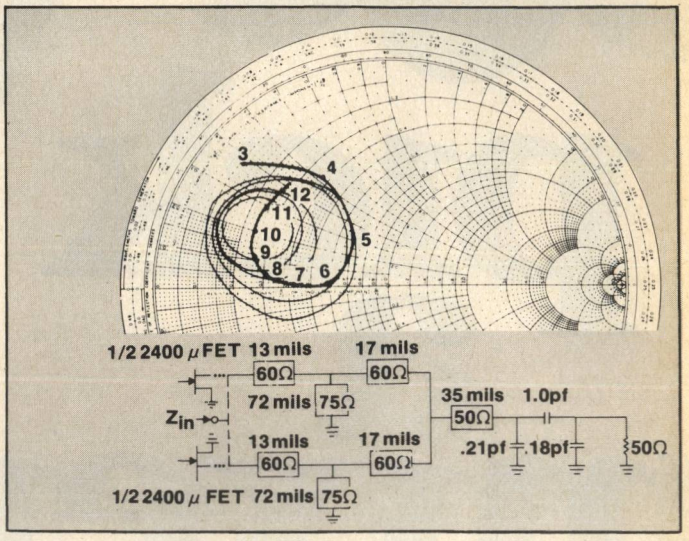

Fig. 5 Optimized output circuit and impedance locus. Shunt capacitor parasitics are also included. The 2400 μm FET is divided into two 1200 μm FETs.

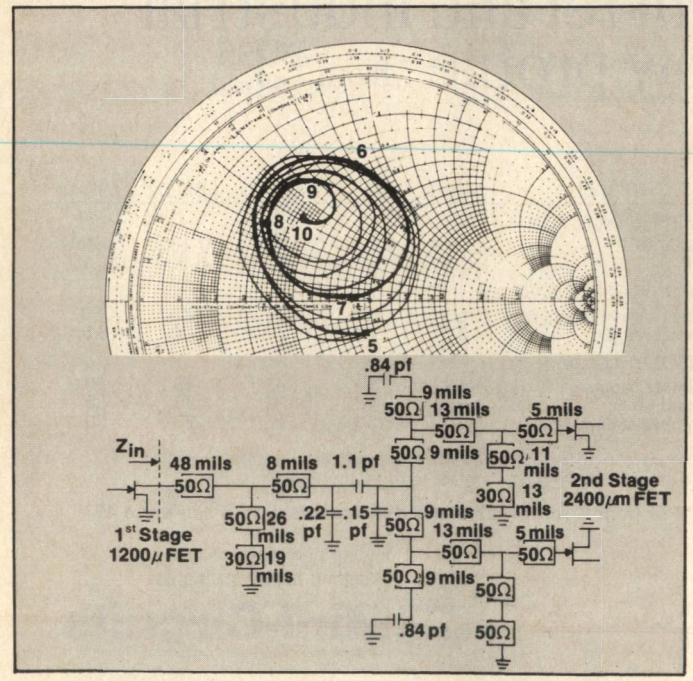

Fig. 6 Optimized interstage circuit and impedance locus. The circuit was derived from a six element lumped circuit.

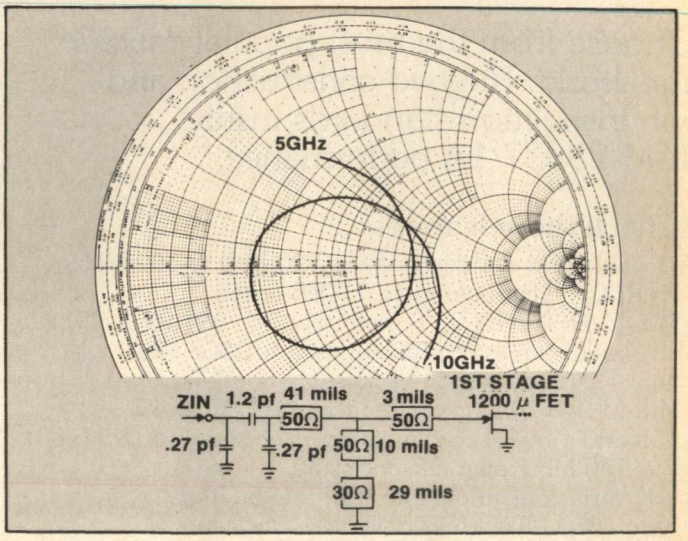

Fig. 7 Final input circuit and associated input match. VSWR is 2:1 from 5 to 10 GHz.

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er algorithm to optimize the impedance locus fit to the composite load-pull contours. Figure 5 shows the final output network, including capacitor parasitics and the associated impedance locus. Note that the 2400 μm FET has been accurately modeled as two parallel 1200 μm FETs since the actual circuit incorporates a ground via at the center of the 2400 μm FET. See Figure 8a.

The same technique is applied to design the interstage circuit. In this case, however, the impedance to be transformed is the complex RC input impedance of the 2400 μm FET. Figure 6 shows the final optimized interstage network, including capacitor parasitics, and the corresponding transformed impedance locus. Although the network appears complex, it was derived from a rather simple six element lumped circuit. Notice again that the topology chosen provides convenient biasing for the gate of the 2400 μm FET and drain of the 1200 μm FET through shunt inductors and off-chip bypass capacitors. DC isolation between the two FETs is provided by a series capacitor.

All that is left in the amplifier design is to flatly match the 1200 μm FET across the band. There are several commercially available computer programs which can easily accomplish this task once given a circuit topology. Figure 7 shows the final input network and input match. The VSWR is slightly higher than 2:1 across the band which is the best that can be obtained, for the given number of circuit elements, due to the Fano-Bode Limit on matching reactive loads.

Experimental Results

The design procedure discussed above has been used to design several iterations of 5-10 GHz and 8-12 GHz two stage amplifiers employing 1 micron gatelength FETs. Figure 8a shows the latest 5-10 GHz amplifier incorporating a 1200 μm FET (four 300 μm cells) in the first stage and 2400 μm FET in the second stage. Overall amplifier substrate size is .080" x .200" x .004" thick. The matching circuits incorporate interdigital capacitors (5 μm fingers and 5 μm gaps) and inductors formed by short lengths of high impedance microstrip transmission lines. Airbridges and via holes are used, respectively, to interconnect the FET source pads and to provide low inductance source grounds. The via holes also improve circuit layout flexibility by permitting grounding of circuit elements to the chip. For this amplifier RF bypassing is accomplished using off-chip capacitors located adjacent to the amplifier. These capacitors also provide a convenient means for injecting bias. Overlay capacitors are being used in designs currently in processing to shrink the circuit size as well as allow for RF bypassing on the amplifier substrate.

The performance of this amplifier is shown in Figure 8b. Power output is 1 watt from approximately 5.5-9.0 GHz with 9 dB associated gain. The roll off at 10 GHz is due to the gates being slightly longer ($\approx$1.2 μm) than desired.

An 8-12 GHz two stage amplifier was also designed and fabricated using the 1 μm gatelength FETs shown in Figure 8. These FETs are not optimum for 12 GHz operation, and the amplifier was predicted to have only about 1/2 watt output based on load pull measurements on individual 1200 μm FETs. Power output for this 8-12 GHz amplifier was measured to be 400-500 mW over the 8-12 GHz band with 7 dB associated gain.

3 W Four Stage 8-12 GHz Amplifier

The design goals for Phase II of the aforementioned program were expanded to a four stage, 8-12 GHz monolithic amplifier capable of producing 3 watts. Associated power gain was set at 18 dB. A key element to the success of this phase is the development of submicron (0.7 μm) gate technology using deep UV photolithographic techniques. Special circuit design techniques must also be developed to meet the power and bandwidth goals.

In order to achieve the 3W output power goals for the four stage amplifier, it is necessary to employ a large gate width ($\approx$6400 μm)

FET in the final amplifier stage. Directly paralleling thirty-two 200 μm cells, for example, in order to obtain the required 6400 μm total gate periphery results in an extremely low FET input impedance. Matching an impedance this low (1 to 2Ω) to 50Ω over a broad bandwidth is exceedingly difficult. More importantly, in a FET this large, phase differences between the cells close to the center feed point and those farthest away from the feed point cause a significant reduction in FET gain and power output. THis is particularly true at X-band frequencies and above.

An alternative to direct cell combining through the use of a "cell cluster matching" design approach is shown in Figure 9. In this approach, cells are grouped together into eight separate 800 μm cell clusters. The amplifier shown is the first iteration of a single stage design which is power matched at both the input and output across the 8-12 GHz band (i.e. no gain slope compensation is used). Note that this matching is done at the 800 μm cell cluster level where the input impedance levels are high. Each cell cluster is partially matched before combining, thereby resulting in an overall higher impedance level at the combining points and a corresponding improvement in performance over a broad bandwidth. Each cell cluster is first "double tuned" to a "convenient" resistive impedance level and combined with another partially matched cell cluster. A $\lambda/4$ transformer then transforms the combined resistive impedance level of each of the four cluster pairs to 200Ω. A "convenient" impedance level is defined as one which allows a practical line impedance to be used as the $\lambda/4$ transformer while not serverely complicating the initial double tuning circuitry. The four cell cluster pairs, now transformed to 200Ω, are combined to produce the desired 50Ω match.

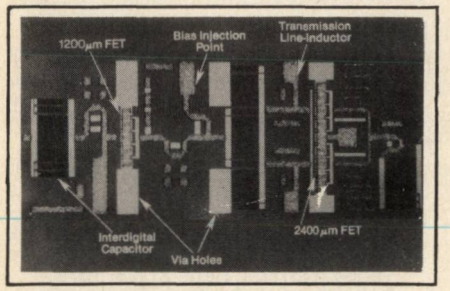

Fig. 8a 5-10 GHz 1 Watt amplifier.

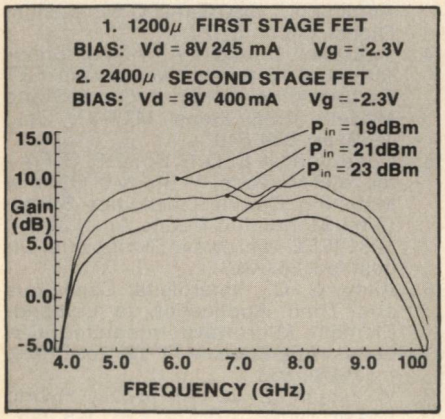

Fig. 8b Measured performance of amplifier.

Note that since the cell cluster matching circuits are identical, the phase angles of the wavefronts reaching each cluster are identical thereby eliminating intercell phasing problems. Figure 11 shows an example of the impedance progression just described on the output or drain side of a single stage, 3 W amplifier using four 1600 μm cell clusters. The intermediate impedance level in this design is 17Ω corresponding to a 59Ω $\lambda/4$ transformer.

By placing resistors, whose values are equal to the resistive impedance level looking into each partially matched cell cluster pair, at the ends of each $\lambda/4$ line and tying the other end of each resistor to a common node, a four way Wilkinson power combiner/splitter is formed.[7] This type of combiner has good isolation characteristics over reasonably broad bandwidths. This isolation reduces cell to cell interactions and thereby minimized amplifier performance degradation due to cell to cell variation. Unfortunately, on a planar structure, such as a monolithic amplifier, long inductive line lengths and air bridges must be used to connect the isolation of the combiner to decrease with increasing frequency. To eliminate this effect, we have added series capacitors at the centers of each connecting line to resonate out the inductive effects at midband (10 GHz) and better approximate a short circuit. However, isolation with 50Ω resisitors is

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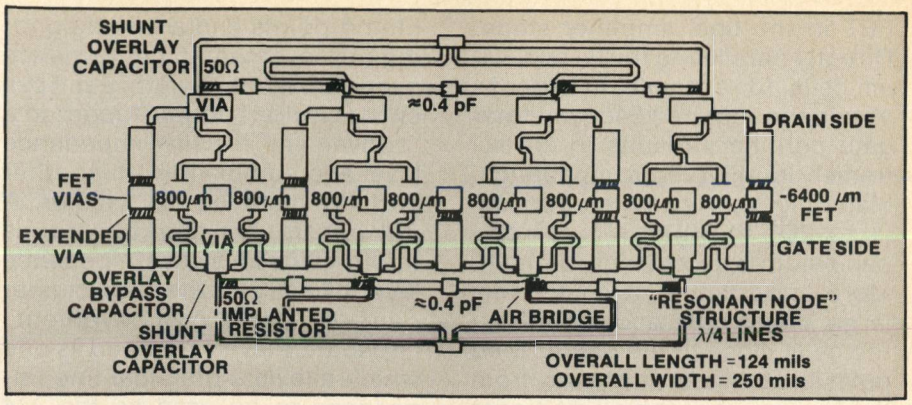

Fig. 9 8-12 GHz, 3 Watt amplifier layout using the "cell cluster matching" approach described. Calculated small signal gain is 8 dB.

improved as much as 10 dB over the no isolation resistor case.

This amplifier is in fabrication at the time of this writing. Therefore, no test data is available. However, calculated small signal gain, of the amplifier, averages around 8.2 dB from 8-12 GHz. Input and output return losses, for power matched conditions are better than 10 dB.

Summary

The future production of low cost, high performance monolithic amplifiers and devices is dependent upon the development of key fabrication and circuit design technologies. Direct selective ion implantation into high purity LEC grown semi-insulating GaAs substrates was discussed as a key fabrication technology. An area conserving amplifier design technique was detailed that achieves a good input match, high output power and broad bandwidth without the need for relatively large monolithic quadrature couplers. Experimental results were shown for a 1W, 5-10 GHz amplifier designed with this technique.

Finally, a design approach was described for a 3W, 8-12 GHz amplifier that addresses the three main problems associated with large periphery power FETs. Namely, the problems of:

- matching to low impedance levels over broad bandwidths,
- ensuring equal power and phase to each cell cluster, and
- eliminating inter-cell interactions through the use of the "resonant node" isolation structure.

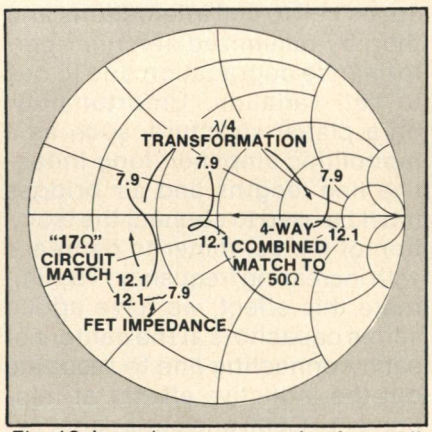

Fig. 10 Impedance progression for a cell cluster matched 3W design using four 1600 μm cell clusters.

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Computer Aided Design And Manufacture Of GaAs Hyperabrupt Varactors

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Introduction

Since the early 60's silicon voltage variable capacitance (varactor) diodes have been available; gallium arsenide varactors became available in the 70's These GaAs diodes initially were used in specialty applications in which higher Q was necessary to obtain lower loss circuit performance. As advances in technology occurred, the use of GaAs varactor diodes in non-specialty and volume applications became feasible.

For p-n junctions, the dependance of junction capacitance, Cj, on applied voltage, V, is given by:

$$C_J(V) = \frac{C_{JO}}{(1 + \frac{V}{\phi})^{\gamma}}$$

where

ϕ = the built-in potential (= 1.3 volts for GaAs)

C_{JO} = a constant (mathematically equal to the junction capacitance when V =0)

γ = the capacitance-voltage slope exponent (gamma).

For the normal abrupt junction p+/n varactor, made by forming a p+ junction on uniformly doped n type semiconductor material, gamma is approximately equal to 0.5. A varactor is called "hyperabrupt" when $\gamma > 0.5$. This larger value of γ indicates that the capacitance changes more rapidly with voltage for a hyperabrupt varactor than for an abrupt varactor. However, most commercially available hyperabrupt varactors are not characterized by a constant value of γ and the value of γ varies widely with applied voltage.

In practice, GaAs varactors are used in the following types of applications:

- high Q abrupt junction tuning varactors,
- constant γ hyperabrupt tuning varactors for tuning linearization,
- maximum C-swing hyperabrupt tuning varactors, and
- low distortion hyperabrupt tuning varactors.

There is an infinite number of GaAs varactors, C_{JO} and γ combinations, based on the profile and area. However, using computer technology it is practical to design and manufacture a varactor diode for each particular circuit application. This paper illustrates the selection, design and manufacture of a GaAs varactor diode. Selected for illustration is a constant γ GaAs hyperabrupt varactor, although the method is applicable to any varactor.

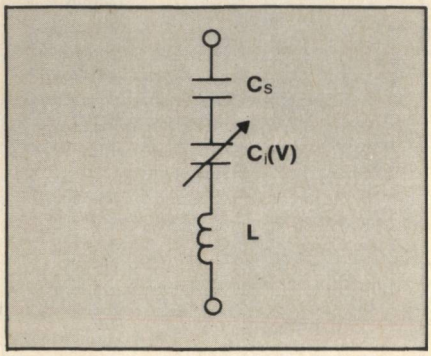

Fig. 1 Series resonant circuit.

Circuit Considerations

The varactor design begins with the circuit function. We use as an illustration, a constant γ hyperabrupt varactor required to give linear frequency tuning of a voltage controlled oscillator (VCO) (without the use of a separate linearizer circuit). For a simple resonant circuit comprised of an inductance, L, and the varactor junction capacitance Cj (V), the frequency-voltage relationship is given by:

$$f_r(V) = \frac{1}{2\pi\sqrt{LC_j(V)}} = \frac{1}{2\pi\sqrt{LC_O}}\left(1+\frac{V}{\Phi}\right)^{\gamma/2}$$

From this it can be seen that linear frequency versus voltage is obtained if γ is 2.0. However, in nearly all microwave circuits, the varactor is not the only capacitance in the resonator; the capacitance of the active element (Cj) is only a portion of the capacitance of the complete resonant

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structure. An analysis has been performed of the simple series circuit illustrated in Figure 1 wherein a fixed capacitance, C_s, is used in series with the varactor. The results of this analysis provide guidance to the selection of a suitable γ for the circuit designer. The resultant total capacitance, C_T, of the resonant circuit can be expressed in terms of a coupling factor, K_s, as:

$$\frac{1}{C_T(V)} = \frac{1}{C_{TO}}\left[1 - K_S + K_S\left(1 + \frac{V}{\Phi}\right)^{\gamma}\right]$$

where:

$$K_s = \frac{C_{TO}}{C_{JO}}$$

When $K_s = 1$, the varactor is fully coupled and the corresponding optimum value for $\gamma = 2$. when K_s approaches 0, the varactor becomes very decoupled, reduced band frequency tuning is possible, and the optimum γ is about 1.0. For intermediate values of coupling, in the range $0 < K_s < 1$, an optimum value of constant γ for linear frequency tuning is predictable for any particular tuning bandwidth. The result of the analysis is illustrated in Figure 2. The optimum γ value is plotted versus the tuning frequency ratio, $R = f_{max}/f_{min}$ with the coupling factor K_s, as a parameter. Notice that linear tuning can be achieved for constant gamma within the limits $1.0 < \gamma < 2.0$, depending on the coupling factor.

The circuit designer can use this analysis for selection of constant gamma hyperabrupts. For example, suppose that the circuit specification requires a tuning ratio of 2:1; the designer could select $\gamma = 2$ and fully couple the varactor with $C_{max}/C_{min} \geq 4$. Alternatively, he could decouple to $K_s = 0.6$, for which he should select $\gamma = 1.6$ and $C_{max}/C_{min} \geq 6$. Even further decoupling could be selected to improve resonator Q with correspondingly lower bandwidth and γ. The decoupling limit occurs when the C_{max}/C_{min} is not realizable in the varactor. Most broadband tuning requirements are optimized in user circuits with $1.2 < \gamma < 1.4$ while circuits with narrow tuning bandwidths utilize a value of γ near 1.0.

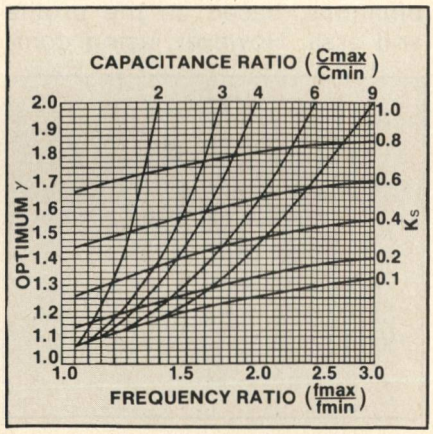

Fig. 2 Optimum γ selection for linear tuning.

This anaylsis determines the capacitance voltage curve required of the diode, that is, the value of γ and the range of voltage over which this value of γ is required. To relate these requirements to the requisite material specifications, it is also necessary to specify the minimum breakdown voltage (V_B) required. This is done by considering the maximum control voltage V and adding some safety margin to insure against breakdown or nonlinearity with RF drive, either of which could cause circuit noise and/or tuning instability.

Computer Aided Device Design

Establishing the proper epitaxial material characteristics is done by starting with an assumed set of parameters, testing them mathematically, using the computer model, then modifying the starting set appropriately in a multipass algorithm. A computer program was developed to determine a unique set of material characteristics for fabrication of devices of specified C(V) and breakdown voltage, V_{BR}, without prior knowledge of the final device area.

The logic flow diagram for the computer aided device design program is shown in Figure 3. Also indicated is the computer aided measurement branch of the program, to measure the finished diode. From the measurements, the material parameters actually realized can be calculated as a check on the initial design.

The computer program provides flexibility in data input for design. Specified device parameters may be entered for the packaged device and chip de-embedding (subtraction of package capacitance) performed as required. Capacitance-voltage data can be entered in the form of discrete points or using one C(V) point and a set of voltage-gamma points. Generation of the overall C(V) for analysis is performed in either of two methods. Conventionally linear interpolation between the input data points is used. The second method allows C(V) generation by piecewise constant gamma interpolation, the more practical of the two because it avoids pronounced inflections in the C(V) curve.

Following the generation of the high resolution capacitance-voltage data array, an initial impurity concentration profile is generated for a unit area device, by applying the following relations:

$$N(x) = \frac{C(V)^3}{q\,\varepsilon\,A^2}\left[\frac{dC(V)}{dV}\right]^{-1}$$

and,

$$x = \frac{\varepsilon A}{C(V)}$$

where A is the device area, q is the electronic charge, ε is the permittivity of the material and x is the distance from the junction. The resulting impurity concentration profile is then numerically integrated to obtain the electric field distribution: E(x):

$$E(x) = \frac{q}{\varepsilon}\int_0^{\omega} N(x)dx$$

where ω is the maximum extent of the depletion region at breakdown. At this point, the data is tested for conformance to the input V_{BR} by performing the ionization integral over the electric field distribution.

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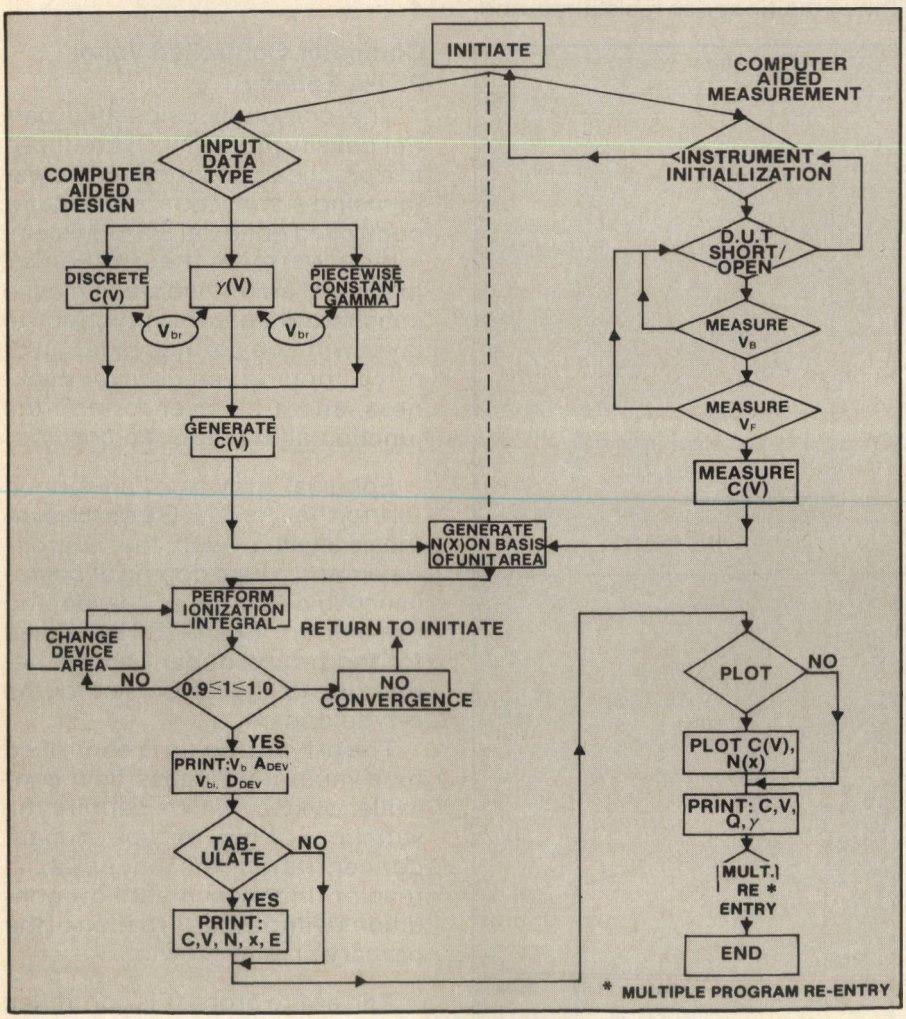

Fig. 3 Logic flow diagram for material design.

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$$I=\int_0^{\omega}\alpha_n(E)\exp\left[-\int_0^{x}\left\{\alpha_n(E)-\alpha_p(E)\right\}dx'\right]dx$$

where $\alpha_n(E)$ and $\alpha_p(E)$ are the electric field dependent ionization rates for electrons and holes, respectively. For I greater than unity, the device area is adjusted upward and the impurity concentration profile recalculated. This procedure is iterated until

$$0.9 \leq I \leq 1.0$$

to insure meeting the specified breakdown voltage.

The design data available at this phase of the program are the impurity concentration profile, device area, and minimum GaAs epitaxial layer thickness. The quality factor, or Q, of the device may now be optimized using

$$Q = \frac{1}{\omega R_S C_S}$$

were ω is the radian frequency (conventionally 2π 50 MHz), R_S is the parasitic series resistance, and C_S is the device capacitance. The contributions to R_S arise from resistivity of the metallization, substrate, buffer-layer and junction-layer resistance and the undepleted epitaxial material, R_{ud}, given by:

$$R_{ud}(V) = \int_{x(V)}^{t_A} \frac{dx}{q\mu N(X)A}$$

where t_A is the total n-layer thickness, x (V) is the depletion depth at voltage V (conventionally, 4 volts) and μ is the electron mobility. Q optimization proceeds from the above relations on the basis of reduction of total n-layer thickness as well as by increasing N(x) within the constraint of minimum breakdown voltage.

Data output occurs following the above analytical phases of the program. An example of the graphical output for material for a constant gamma hyperabrupt tuning varactor is shown in Figure 4.

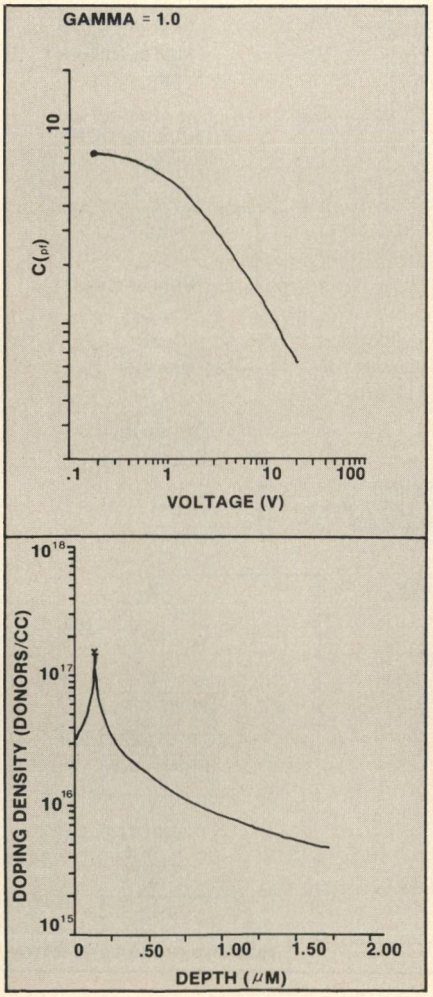


Fig. 4 Constant γ material device design.

Computer Controlled Vapor Phase Epitaxy

The computer calculated carrier density profile [N(x)] is reduced to a practical semiconductor crystal using a subsequent computer controlled eptiaxial GaAs system, which permits the sequential growth of an n+ layer to minimize substrate effects, the n-type active layer with the correct variation of n-type doping versus layer thickness, and a p+ layer to form the junction at the required position.

Epitaxial growth is performed using the $AsCl_3/GaAs/H_2$ synthesis system with the appropriate n and p type doping accomplished by control of the doping gas mixture. Silane (SiH_4) is used for the n-type dopant and dimethyl zinc $(CH_3)_2Zn$ is used for the p-type dopant.

The n-type doping is controlled by a multi-input mass flow controller system which permits the variation of the n-type dopant concentration in the epitaxial reactor under constant flow conditions without perturbation of the primary crystal growth.

The entire process is controlled by an HP1000 mini-computer and an HP9611R remote subsystem.

Process commands, including switch actuation, flow commands timing and thermal set points are controlled by the computer, and process variable such as actual flows, elapsed time, and measured temperatures are monitored.

To determine what carrier density profile is achieved, it is necessary to model the epitaxial GaAs system response to doping concentration changes. Such modeling includes the growth process response of the epitaxial crystal to changes made in the doping dilution system including the effects of the time interval between the change and the growing crystal response and the effects of diffusion broadening of the changed dopant concentration during this interval.

This correlation between modeling and material growth has been accomplished successfully enough to permit the attainment of sufficiently high yields that volume production of inexpensive varactor diodes in glass packages is feasible even for use in the important commercial VHF and UHF frequency ranges.

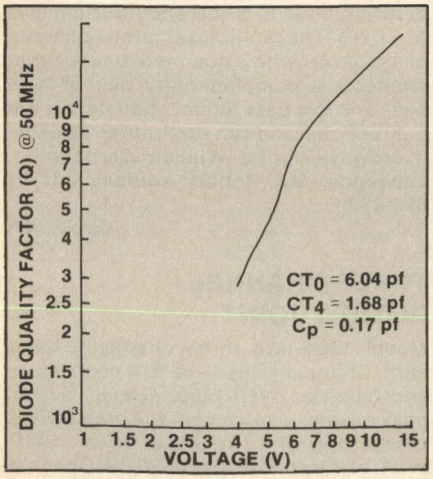


Fig. 5 Device Q vs voltage.

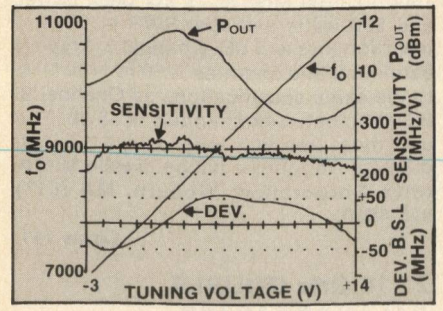


Fig. 6 7-11 GHz FET VCO performance.

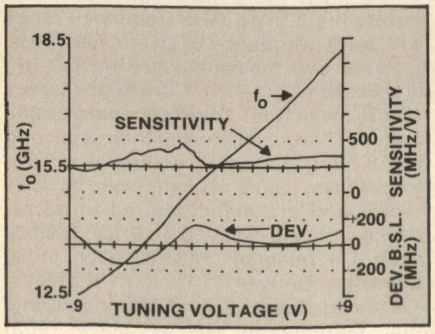


Fig. 7 Dual FET Ku-band VCO performance.

RF Results

Because of the high electron mobility in GaAs, HATV devices fabricated from GaAs can have lower parasitic series resistance, and, therefore higher Q than corresponding silicon diodes. The Q as a function of reverse bias, as measured by the DeLoach method for a GaAs HATV device, is shown in Figure 5. The Q at -4 volts and 50 MHz is approximately 3000 and increases to over 20,000 with increasing voltage.

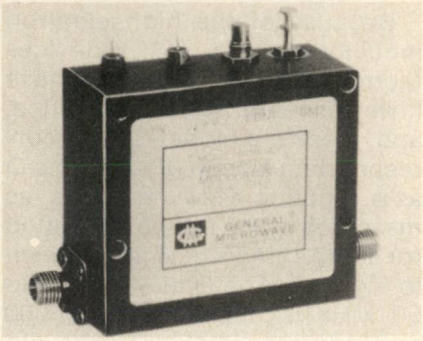
Constant gamma GaAs HATV diodes are useful in both X-band and Ku-band FET VCO's. RF results for a single FET X-band VCO are shown in Figure 6. Modulation sensitivity is essentially constant across the 7 to 11 GHz band. In addition, the deviation of the tuning characteristics from a best-fit straight line (B.S.L.) is a maximum of +50 MHz. Performance data for a dual FET Ku-band VCO from 12.5 to 18.5 GHz are shown in Figure 7. The tuning characteristic deviation from B.S.L. in this case was within ±163 MHz.

The utility of this approach extends to various circuit uses, and troublesome system problems, for example, intermodulation distortion in varactor tuned UHF filters. Use of conventional varactors results in high intermodulation distortion at low bias voltages with reduced distortion at increased bias. With the linear variation of capacitance with voltage in the varactors, intermodulation distortion becomes voltage independent. Specialized varactors have produced UHF filters exhibiting intermodulation distortion of < -30 dB over the voltage bias range while providing frequency tuning from 500-800 MHz. ■

Microwave Products

Components

0.5 - 18 GHz VOLTAGE CONTROLLED ATTENUATORS



A series of three 60 dB voltage controlled attenuators with integrated linearizing drivers cover the frequency range from 0.5 to 18 GHz. Model D1960A operates from 0.5 to 4 GHz, D1962A from 2 to 8 GHz, and D1958 from 8 to 18 GHz. Attenuation can be continuously varied from 0 to 60 dB with a single input control voltage from 0 to 6 volts at a rate of 10 dB/volt. At the 60 dB level, frequency sensitivity is ± 1.6 dB over the full frequency range, and less at lower attenuation levels. At ± 25° C, rated accuracy for Model D1958 is less than ±1.5 dB; and for the lower frequency D1960A and D1962A, within ±2 dB. Built-in temperature compensation circuitry limits temperature coefficients over the operating temperature range from -54° to +110°C to ±0.01 dB/°C up to 8 GHz; and ±0.025 dB/°C up to 18 GHz. The low frequency units measure 2"x 1.8" x .88"; and the high frequency model is 1.25" x 1.25" x .50". **General Microwave Corporation, Farmingdale, NY Moe Wind (516) 694-3600.**

Circle 137.

3-4 GHz ATTENUATOR

Model 4813-15A miniature variable attenuator operates over the 3.0 to 4.0 GHz frequency range with an attenuation range of 15dB. The unit features an attenuation vs frequency specification of better than ±1.0 dB, 1.5 SWR maximum and an insertion loss of 0.5 dB. The attenuator measures 2 x 1½ x ¼ inch and the control mechanism is a multi-turn screwdriver shaft with lock nut. Price $270.00 small quantity price in standard package, with increase variations in price with the panel mount configuration, turns counting configuration or with a micrometer control. **ARRA, Inc., Bay Shore, NY Mike Geraci (516) 231-8400.**

Circle 131.

250 - 500 MHz DIRECTIONAL COUPLER

Model DC-500-BNC directional coupler may be used to sample transmitter or signal generator power from 250 to 500 MHz. The 50 ohm unit has a nominal SWR of 1.1, with a line loss of less than .2 dB. Line input power rating is 50 W maximum CW, and coupling loss is 30 ± 3.5 dB. Directivity is 10 dB minimum over the band. The unit measurers 2.5" x 1.5" x 1" excluding connectors. Price: $60.00 each 1-9 quantity. Delivery: stock to 30 days ARO. **Elcom Systems Inc., Boca Raton, FL Leonard Pollachek (305) 994-1774.**

Circle 135

0.25 - 18 GHz MULTIPLEXERS

Series W-1800 broadband multiplexers are available in frequencies from 0.25 to 18 GHz. The units feature suspended substrate technology for separating and combining octave bandwidth signals with stop band isolation to 60 dB and insertion loss to 1.0 dB. The multiplexer circuit consists of a diplexer with a common junction that connects a complimentary pair of high pass and low pass filters. Multiplexers are bidirectional and can separate or combine microwave signals. **Wincom Corporation, Lawrence, MA Robert Antonucci (617) 685-3930.**

Circle 147.

THREE CHANNEL ROTARY JOINT

Model 1384 is a three channel L-band joint. Channel 1 has 1-5/8 EIA connectors and operates 1250-1400 MHz at 750 kW peak power and 4 kW average power while pressurized with 15 PSIG of dry air. SWR is 1.1, and insertion loss is .25 dB. Channel 2 has N type connectors and operates 1000 to 1100 MHz at 15 kW peak power and 500 watts average. SWR is 1.3 and insertion loss is .5 dB. Channel 3 is type N connector and operates 1250 to 1400 MHz to the same specifications as Channel 2. Isolation between channels is 55 db. The unit measures 30" long with a 17 inch diameter mounting flange. **Kevlin Microwave Corporation, Woburn, MA (617) 935-4800.**

Circle 141.

2 - 18 GHz DOUBLE BALANCED MIXER

Model MDS 285 double balanced mixer covers the 2 to 18 GHz frequency range with an IF frequency of DC to 1000 MHz. Isolation over the band is 23 dBm (LO-RF) and 30 dBm (LO—IF). Conversion loss is 12 dB maximum. The 1dB compression point is +3dBm, third order intercept point is +16 dBm. LO power required is +5 dBm to +13 dBm. Units operate over -55° C to +85° C and are manufactured in accordance with MIL-STD-202E. Price: $590.00 each 1-4 quantity, $439.00 each in 50 quantity. Delivery: stock to 4 weeks. **Technical Research and Manufacturing, Inc., Manchester, NH Art Marin (603) 668-0120.**

Circle 149.